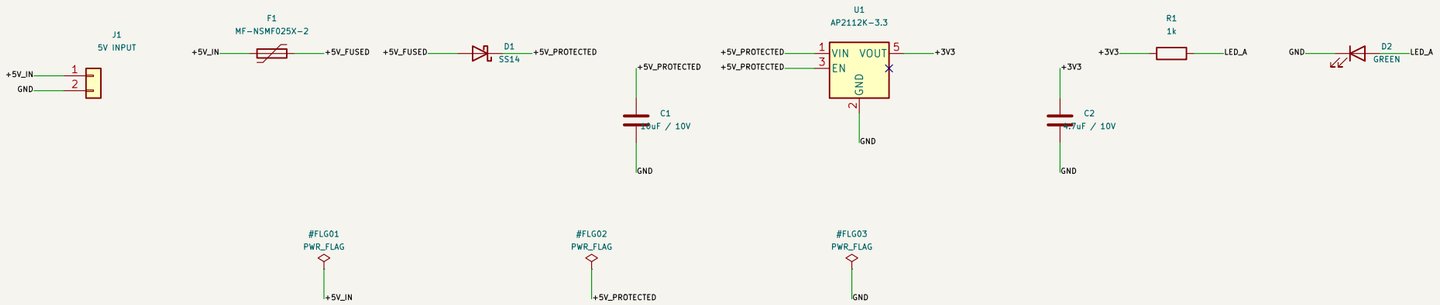
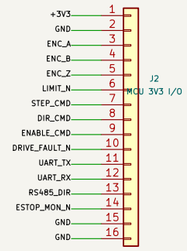
1 | PROTECTED LOGIC SUPPLY



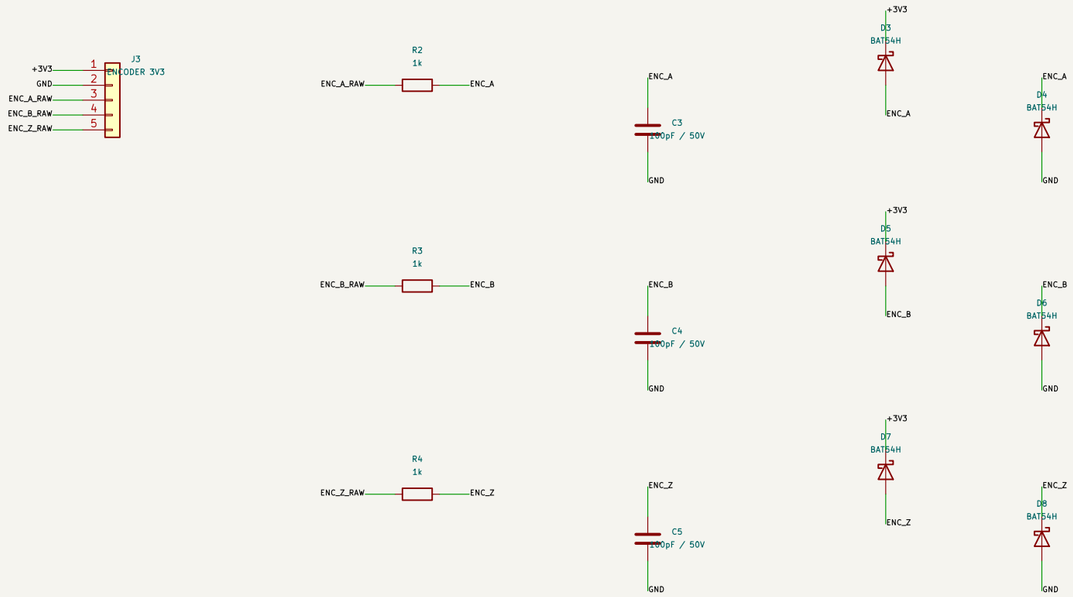
5.0 V +/-5% regulated source. 3.3 V total load budget <=150 mA.
PWR_FLAG: external source / diode-passive source declaration.
C1/C2 X7R: effective output capacitance >=1 uF after DC bias.

2 | EXTERNAL MCU / LOGIC CONTRACT



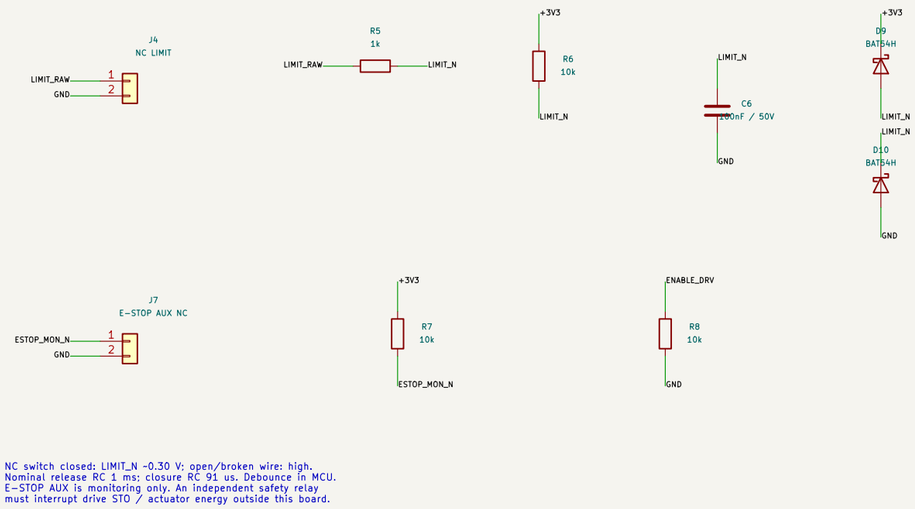
MCU is external; signal directions in electronics documentation.
GPIO must have Schmitt inputs on ENC_* and LIMIT_N.
3.3 V supply is an output: do not back-power this interface.

3 | QUADRATURE ENCODER INPUTS



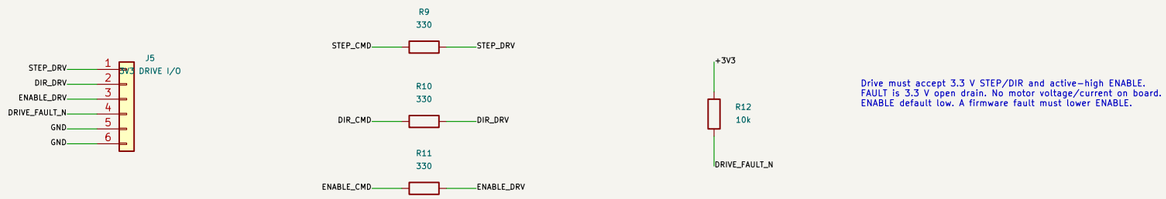
3.3 V push-pull / open collector encoder only; add source pull-ups
for open collector. RC nominal 100 ns; selected as an educational
short-cable interface. Clamp diodes provide limited surge protection.
Cable ESD / EMC, hysteresis and edge timing need physical verification.

4 | LIMIT + E-STOP MONITOR



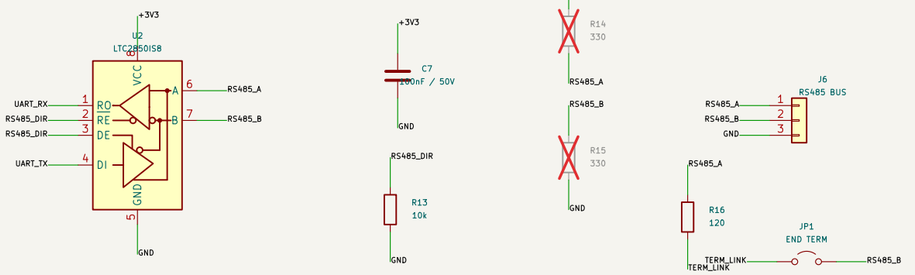
NC switch closed: LIMIT_N ~0.30 V; open/broken wire: high.
Nominal release RC 1 ms; closure RC 91 us. Debounce in MCU.
E-STOP AUX is monitoring only. An independent safety relay
must interrupt drive STO / actuator energy outside this board.

5 | EXTERNAL DRIVE COMMAND



Drive must accept 3.3 V STEP/DIR and active-high ENABLE.
FAULT is 3.3 V open drain. No motor voltage/current on board.
ENABLE default low. A firmware fault must lower ENABLE.

6 | HALF-DUPLEX RS-485



R14/R15 DNP by default: LTC2850 has internal receiver failsafe.
Optional bias at one node only. JP1 closed only at two bus ends.
250 kbit/s target; non-isolated short bench bus; common ground.
Six joint nodes + gripper node; bus firmware remains conceptual.