PROJECT SCCI RH / INTEGRATED MODULAR CIRCUIT SYSTEM

Eight functional boards; actual mapped electrical connections and physical tap headers.

Reference namespaces preserve frozen source identities. Read integrated-pcb-wiring.csv for the harness.

Common driver rearm and independent supervisor phase rearm are deliberately separated.

Digital artificial-load concept. Geometry and ERC do not establish implantation or measured performance.

monitoring-cell



File: monitoring-cell/monitoring_cell.kicad_sch

current-driver



File: current-driver/current_driver.kicad_sch

recording-front-end



File: recording-front-end/recording_front_end.kicad_sch

contact-router



File: contact-router/contact_router.kicad_sch

supervision



File: supervision/supervision.kicad_sch

power



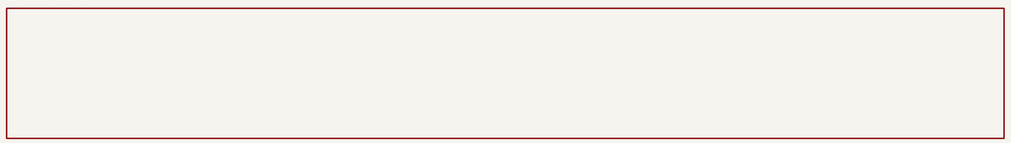
File: power/power.kicad_sch

monitoring-transport



File: monitoring-transport/monitoring_transport.kicad_sch

controller-carrier



File: controller-carrier/controller_carrier.kicad_sch

Project SCCI RH

Sheet: /

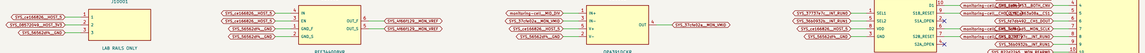
File: SCCI_RH_integrated.kicad_sch

Title: Project SCCI RH / Integrated modular SCCI electrical system

Size: A2	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 1/80

ARTIFICIAL ELECTRICAL LOADS ONLY / FIRST MONITORING SLICE

No current driver. HV router. differential compliance circuit. Independent watchdog. MCU or PCB is completed here.

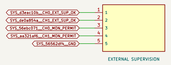


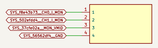












V_REF=4.096V; V_MID=2.048V. Low INT_RUN resets: high opens reset for continuous signed integration.

I_LO=1.04757V / I_HI=3.04843V nominal (−+/−25.01mA). Threshold is NOT a proven complete-waveform cap.

EXT_SUP_OK must stay LOW until external rails/reference/watchdog/compliance/duration checks pass.

Two INA241 channels alone: up to32mW atSV. Input bias25.45uA/input is an unresolved leakage/bypass term.

Named global nets connect sheets; connectors remain explicit external design contracts. Read README before interpretation.

Source0_monitor

File: channel0.kicad_sch

Source1_monitor

File: channel1.kicad_sch

integrated_component_taps

File: integration_taps.kicad_sch

ARTIFICIAL LOADS ONLY; native schematic slice, not a completed implant

Project SCCI RH

Sheet: /monitoring-cell/

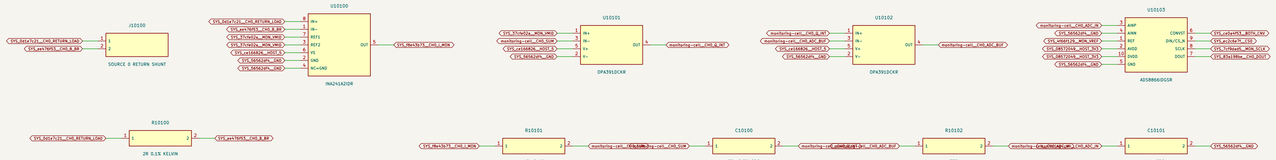
File: monitoring_cell.kicad_sch

Title: Project SCCI RH S4 / Shared reference and interfaces

Size: A1	Date: 2026-10-12	**Rev: 0.2 DCK**
KiCad E.D.A. 10.0.6		Id: 2/80

ARTIFICIAL ELECTRICAL LOADS ONLY / FIRST MONITORING SLICE

No current driver. HV router. differential compliance circuit. independent watchdog. MCU or PCB is completed here.



Qₙ=10k*22n/40*(V_end−V_start): 600nC=109.091mV nominal. Take BASELINE, CATH. ANODE, NET/TAIL endpoints.

Cathodic and anodic charges remain separate. Opposed phases can cancel: final net alone cannot qualify delivery.

Actual current-tail/window evidence is required. Command edges. the comparator or an ideal16-bit LSB do not certify precision.

CLRN = HI_OK AND LO_OK AND EXT_SUP_OK. Any low latches Q off: rising REARM admits only while CLRN is high.

ARTIFICIAL LOADS ONLY; native schematic slice, not a completed implant

Project SCCI RH

Sheet: /monitoring-cell/Source0_monitor/

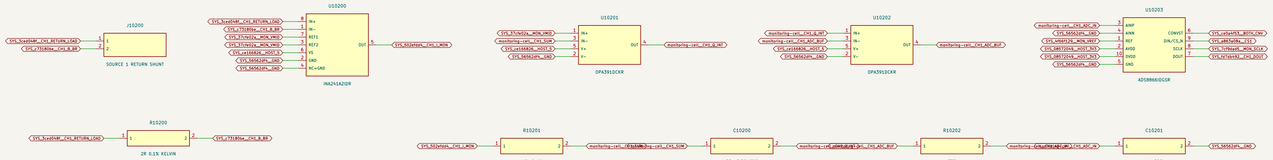
File: channel0.kicad_sch

Title: Project SCCI RH S4 / Source 0: current and phase charge

Size: A1	Date: 2026-10-12	**Rev: 0.2 DCK**
KiCad E.D.A. 10.0.6		Id: 3/80

ARTIFICIAL ELECTRICAL LOADS ONLY / FIRST MONITORING SLICE

No current driver. HV router. differential compliance circuit. Independent watchdog. MCU or PCB is completed here.



Q=−10k*22n/40*(V_end−V_start): 600nC=109.091mV nominal. Take BASELINE, CATH. ANODE, NET/TAIL endpoints.

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Actual current-tail/window evidence is required. Command edges. the comparator or an ideal16-bit LSB do not certify precision.

CLRN = HI_OK AND LO_OK AND EXT_SUP_OK. Any low latches Q off: rising REARM admits only while CLRN is high.

ARTIFICIAL LOADS ONLY: native schematic slice, not a completed implant

Project SCCI RH

Sheet: /monitoring-cell/Source1_monitor/

File: channel1.kicad_sch

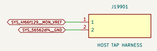
Title: Project SCCI RH S4 / Source 1: current and phase charge

Size: A1	Date: 2026-10-12	**Rev: 0.2 DCK**
KiCad E.D.A. 10.0.6		Id: 4/80

INTEGRATED COMPONENT-TAP HARNESS / monitoring-cell

Physical headers expose actual earlier component taps. Original connectors remain available.

Only named electrical nets connect. AFE, HOST and companion grounds remain distinct.



Artificial-load digital design. Added wiring capacitance and connector integrity require measurement.

Project SCCI RH

Sheet: /monitoring-cell/integrated_component_taps/

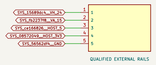
File: integration_taps.kicad_sch

Title: Project SCCI RH / monitoring-cell integration taps

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 5/80

ARTIFICIAL LOADS ONLY / RESTRICTED 24 V, 3 mA, 200 us DRIVER SLICE

External rails, recording AFE, 16-contact routing, compliance, charge guard, watchdog, PCB and implant qualification remain outside.







Source0_analog

File: source0.kicad_sch

Source0_permission

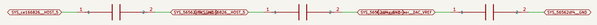
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Source1_analog

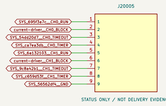
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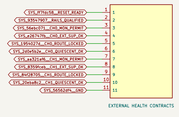
Source1_permission

File: permission1.kicad_sch











DAC initialization before READY: GAIN[0x04]=0x0103, reference divider 2 and both output buffer gains 2 => nominal 2.5 V FSR.

Code 7864 -> 2.99987B mA nominal through 100 ohm. Zero code is not terminal disconnection. Read README and external contracts.

RESET_READY held LOW through startup; REARM is an explicit pulse with REQUEST/TIMER LOW and independently observed quiescence.





Native circuit slice: artificial loads only; no PCB or implant qualification

Project SCCI RH

Sheet: /current-driver/

File: current_driver.kicad_sch

Title: Project SCCI RH S4 / Dual setpoint and external contracts

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 6/80

ARTIFICIAL LOADS ONLY / RESTRICTED 24 V, 3 mA, 200 us DRIVER SLICE

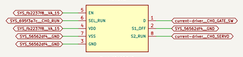
External rails, recording AFE, 16-contact routing, compliance, charge guard, watchdog, PCB and implant qualification remain outside.

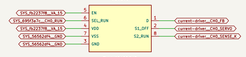


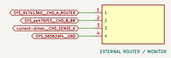




Current path: VH -> upper switch -> artificial pair load + external 2 ohm monitor -> lower switch -> BSP89 -> 100 ohm -> GND.







RUN low grounds gate and closes local unity feedback. RUN high selects current loop. DNP compensation needs a transient study.

























Bridge uses captured direction: all four commanded off during inhibit. Analog rail clamps, input bias and stuck switches remain real paths.

Native circuit slice: artificial loads only; no PCB or implant qualification

Project SCCI RH

Sheet: /current-driver/Source0_analog/

File: source0.kicad_sch

Title: Project SCCI RH S4 / Source 0: regulated sink and polarity bridge

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 7/80

ARTIFICIAL LOADS ONLY / RESTRICTED 24 V, 3 mA, 200 us DRIVER SLICE

External rails, recording AFE, 16-contact routing, compliance, charge guard, watchdog, PCB and implant qualification remain outside.

U20300

LTC6993HS6-1#TRPBF

U20301

SN74LVC1G86DBVR

U20302

SN74LVC1G11DBVR

U20303

SN74LVC1G11DBVR

U20304

SN74LVC1G08DBVR

U20305

SN74LVC1G04DBVR

U20306

SN74LVC1G04DBVR

U20307

SN74LVC1G08DBVR

U20308

SN74LVC1G04DBVR

U20309

SN74LVC1G08DBVR

U20310

SN74LVC1G11DBVR

U20311

SN74LVC1G11DBVR

U20312

SN74LVC1G04DBVR

U20313

SN74LVC1G74DCUR

U20314

SN74LVC1G32DBVR

U20315

SN74LVC1G74DCUR

U20316

SN74LVC1G74DCUR

U20317

SN74LVC1G11DBVR

U20318

SN74LVC1G11DBVR

U20319

SN74LVC1G08DBVR

U20320

SN74LVC1G08DBVR

C20300

100n 10V

C20301

100n 10V

C20302

100n 10V

C20303

100n 10V

C20304

100n 10V

C20305

100n 10V

C20306

100n 10V

C20307

100n 10V

C20308

100n 10V

C20309

100n 10V

C20310

100n 10V

C20311

100n 10V

C20312

100n 10V

C20313

100n 10V

C20314

100n 10V

C20315

100n 10V

C20316

100n 10V

C20317

100n 10V

C20318

100n 10V

C20319

100n 10V

C20320

100n 10V

R20300

175.8k 0.1%

R20301

976k 0.1%

R20302

182k 0.1%

R20303

10k

R20304

10k

R20305

10k

R20306

10k

R20307

10k

R20308

10k

R20309

10k

R20310

10k

BASE_GOOD=MON & EXT & ROUTE & READY & RAILS & XOR(raw directions). Raw REQUEST clocks TIMER; SAFE_REARM preloads direction while off.

Normal request end consumes BLOCK; TIMEOUT records held request at timer fall. REARM requires request/timer LOW + QUIESCENT_OK.

Static/event checks do not qualify asynchronous hazards, supply ramps, propagation delay or real current tails. No automatic retry.

Native circuit slice; artificial loads only; no PCB or implant qualification

Project SCCI RH

Sheet: /current-driver/Source0_permission/

File: permission0.kicad_sch

Title: Project SCCI RH S4 / Source 0: independent duration and sticky admis

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 8/80

ARTIFICIAL LOADS ONLY / RESTRICTED 24 V, 3 mA, 200 us DRIVER SLICE

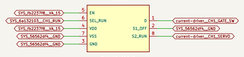
External rails, recording AFE, 16-contact routing, compliance, charge guard, watchdog, PCB and implant qualification remain outside.

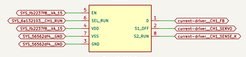


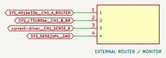




Current path: VH -> upper switch -> artificial pair load + external 2 ohm monitor -> lower switch -> BSP89 -> 100 ohm -> GND.







RUN low grounds gate and closes local unity feedback. RUN high selects current loop. DNP compensation needs a transient study.

























Bridge uses captured direction: all four commanded off during inhibit. Analog rail clamps, input bias and stuck switches remain real paths.

Native circuit slice: artificial loads only; no PCB or implant qualification

Project SCCI RH

Sheet: /current-driver/Source1_analog/

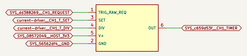
File: source1.kicad_sch

Title: Project SCCI RH S4 / Source 1: regulated sink and polarity bridge

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 9/80

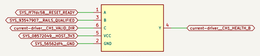
ARTIFICIAL LOADS ONLY / RESTRICTED 24 V, 3 mA, 200 us DRIVER SLICE

External rails, recording AFE, 16-contact routing, compliance, charge guard, watchdog, PCB and implant qualification remain outside.

















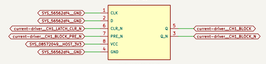




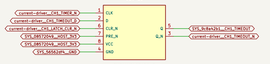


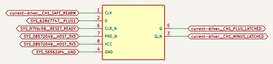


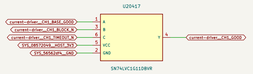
















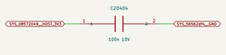








































BASE_GOOD=MON & EXT & READY & RAILS & XOR(raw directions). Raw REQUEST clocks TIMER; SAFE_REARM preloads direction while off.

Normal request end consumes BLOCK; TIMEOUT records held request at timer fall. REARM requires request/timer LOW + QUIESCENT_OK.

Static/event checks do not qualify asynchronous hazards, supply ramps, propagation delay or real current tails. No automatic retry.

Native circuit slice; artificial loads only; no PCB or implant qualification

Project SCCI RH

Sheet: /current-driver/Source1_permission/

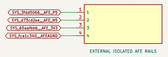
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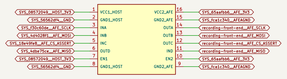
Title: Project SCCI RH S4 / Source 1: independent duration and sticky admi

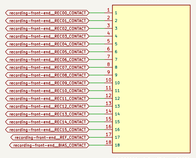
Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 10/80

DIGITAL RESEARCH CIRCUIT / ARTIFICIAL SIGNALS / NO PCB OR IMPLANT QUALIFICATION

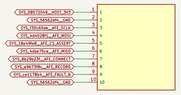
Spinal concept: 16 positive contacts + 1 shared reference + separate passive bias; amplifier linearity and biological recording remain conditional.

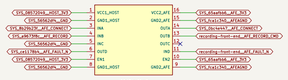




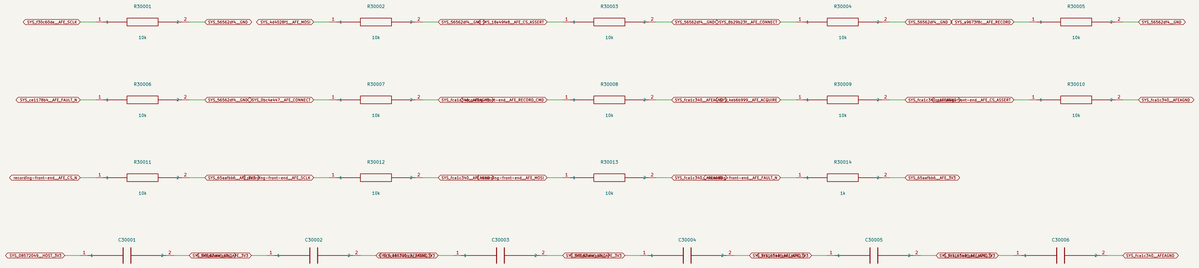












HOSTGND and AFEAGND are separate domains. Both receive valid regulated supplies externally; the digital barrier does not generate power.

acquisition



File: acquisition.kicad_sch

bank0



File: bank0.kicad_sch

bank1



File: bank1.kicad_sch

bank2



File: bank2.kicad_sch

bank3



File: bank3.kicad_sch

reference

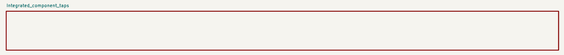


File: reference.kicad_sch

CS_ASSERT low -> Island CS_N high. CONNECT low disconnects HV paths: ACQUIRE = CONNECT & RECORD, so O1 remains clamped.

Driver phase admission needs independently observed ISOLATED_READY; neither commands nor fault flags establish voltage or delivery evidence.

integrated_component_taps



File: integration_taps.kicad_sch

Native digital circuit slice: artificial signals only; external supervisors/power/PCB remain

Project SCCI RH

Sheet: /recording_front_end/

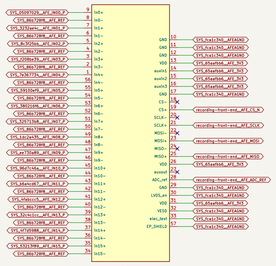
File: recording_front_end.kicad_sch

Title: Project SCCI RH S4 / Isolated SPI, control and supplied power

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 11/80

DIGITAL RESEARCH CIRCUIT / ARTIFICIAL SIGNALS / NO PCB OR IMPLANT QUALIFICATION

Spinal concept: 16 positive contacts + 1 shared reference + separate passive bias; amplifier linearity and biological recording remain conditional.



Every minus input shares AFE_REF. This is 16 differential streams from 18 functional recording ports, not 32 independent recording electrodes.









CMOS mode: LVDS_en=0: negative SPI pins NC; unused aux inputs at VDD: avaout NC; elec_test and VESD at AFEAGND.

Configure, calibrate and verify readback via SPI before valid data. 4MHz / 5us command slots are the revised isolated-link study baseline.

ADC response is pipelined: physical sample timestamps and invalid blanking/recovery intervals must be retained in software.

Native digital circuit slice: artificial signals only; external supervisors/power/PCB remain

Project SCCI RH

Sheet: /recording-front-end/acquisition/

File: acquisition.kicad_sch

Title: Project SCCI RH S4 / RHD2216 / sixteen sampled differential streams

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 12/80

DIGITAL RESEARCH CIRCUIT / ARTIFICIAL SIGNALS / NO PCB OR IMPLANT QUALIFICATION

Spinal concept: 16 positive contacts + 1 shared reference + separate passive bias; amplifier linearity and biological recording remain conditional.

R30100
recording-front-end_REC00_CONTACT
1
2
recording-front-end_REC00_SERIES
4.99k 0.1%

R30101
recording-front-end_REC01_CONTACT
1
2
recording-front-end_REC01_SERIES
4.99k 0.1%

R30102
recording-front-end_REC02_CONTACT
1
2
recording-front-end_REC02_SERIES
4.99k 0.1%

R30103
recording-front-end_REC03_CONTACT
1
2
recording-front-end_REC03_SERIES
4.99k 0.1%

R30200
recording-front-end_REC00_PROT
1
2
SYS_fca12k5_AFEAGND
10M

R30201
recording-front-end_REC01_PROT
1
2
SYS_fca12k5_AFEAGND
10M

R30202
recording-front-end_REC02_PROT
1
2
SYS_fca12k5_AFEAGND
10M

R30203
recording-front-end_REC03_PROT
1
2
SYS_fca12k5_AFEAGND
10M

U30100
SYS_65ae9bb6_AFE_IN3
SYS_4e6b5999_AFE_ACQUIRE
SYS_9da0506a_AFE_IP3
SYS_d7b1d3ee_AFE_AM3
SYS_fca12k5_AFEAGND
EN
SEL_ACQUIRE
VDD
VSS_NEG
GND
S_RHO
S1_CLAMP
S2_PROTECTED
SYS_05097529_AFE_IN03_P
SYS_fca12k5_AFEAGND
recording-front-end_REC00_PROT
TMUX8219DGKR

U30101
SYS_65ae9bb6_AFE_IN3
SYS_4e6b5999_AFE_ACQUIRE
SYS_9da0506a_AFE_IP3
SYS_d7b1d3ee_AFE_AM3
SYS_fca12k5_AFEAGND
EN
SEL_ACQUIRE
VDD
VSS_NEG
GND
S_RHO
S1_CLAMP
S2_PROTECTED
SYS_3233aeec_AFE_IN03_P
SYS_fca12k5_AFEAGND
recording-front-end_REC01_PROT
TMUX8219DGKR

U30102
SYS_65ae9bb6_AFE_IN3
SYS_4e6b5999_AFE_ACQUIRE
SYS_9da0506a_AFE_IP3
SYS_d7b1d3ee_AFE_AM3
SYS_fca12k5_AFEAGND
EN
SEL_ACQUIRE
VDD
VSS_NEG
GND
S_RHO
S1_CLAMP
S2_PROTECTED
SYS_8c3f2f0b_AFE_IN02_P
SYS_fca12k5_AFEAGND
recording-front-end_REC02_PROT
TMUX8219DGKR

U30103
SYS_65ae9bb6_AFE_IN3
SYS_4e6b5999_AFE_ACQUIRE
SYS_9da0506a_AFE_IP3
SYS_d7b1d3ee_AFE_AM3
SYS_fca12k5_AFEAGND
EN
SEL_ACQUIRE
VDD
VSS_NEG
GND
S_RHO
S1_CLAMP
S2_PROTECTED
SYS_f2088e39_AFE_IN03_P
SYS_fca12k5_AFEAGND
recording-front-end_REC03_PROT
TMUX8219DGKR

C30100
SYS_05097529_AFE_IN03_P
1
2
SYS_fca12k5_AFEAGND
470p C0G 50V

C30101
SYS_3233aeec_AFE_IN03_P
1
2
SYS_fca12k5_AFEAGND
470p C0G 50V

C30102
SYS_8c3f2f0b_AFE_IN02_P
1
2
SYS_fca12k5_AFEAGND
470p C0G 50V

C30103
SYS_f2088e39_AFE_IN03_P
1
2
SYS_fca12k5_AFEAGND
470p C0G 50V

C30200
SYS_9da0506a_AFE_IP3
1
2
SYS_fca12k5_AFEAGND
100n X7R 16V

C30201
SYS_9da0506a_AFE_IP3
1
2
SYS_fca12k5_AFEAGND
100n X7R 16V

C30202
SYS_9da0506a_AFE_IP3
1
2
SYS_fca12k5_AFEAGND
100n X7R 16V

C30203
SYS_9da0506a_AFE_IP3
1
2
SYS_fca12k5_AFEAGND
100n X7R 16V

C30300
SYS_d7b1d3ee_AFE_AM3
1
2
SYS_fca12k5_AFEAGND
100n X7R 16V

C30301
SYS_d7b1d3ee_AFE_AM3
1
2
SYS_fca12k5_AFEAGND
100n X7R 16V

C30302
SYS_d7b1d3ee_AFE_AM3
1
2
SYS_fca12k5_AFEAGND
100n X7R 16V

C30303
SYS_d7b1d3ee_AFE_AM3
1
2
SYS_fca12k5_AFEAGND
100n X7R 16V

Per column: contact -> 4.99k -> quad protected S/D -> protected node -> S2; S1 grounds RHO until ACQUIRE is admitted.

C30020
SYS_9da0506a_AFE_IP3
1
2
SYS_fca12k5_AFEAGND
100n X7R 16V

U30020
SYS_35c1ee57_AFE_CONNECT
SYS_35c1ee57_AFE_CONNECT
SYS_35c1ee57_AFE_CONNECT
SYS_35c1ee57_AFE_CONNECT
SYS_9da0506a_AFE_IP3
SYS_d7b1d3ee_AFE_AM3
SYS_fca12k5_AFEAGND
EP_SHIELD
SEL1
SEL2
SEL3
SEL4
VDD
VSS_NEG
GND
S1_CONTACT
S1_INTERNAL
S2_CONTACT
S2_INTERNAL
S3_CONTACT
S3_INTERNAL
S4_CONTACT
S4_INTERNAL
FF_N
recording-front-end_REC00_SERIES
recording-front-end_REC00_PROT
recording-front-end_REC01_SERIES
recording-front-end_REC01_PROT
recording-front-end_REC02_SERIES
recording-front-end_REC02_PROT
recording-front-end_REC03_SERIES
recording-front-end_REC03_PROT
recording-front-end_AFE_FAULT_N
TMUX7612FRRPR

C30030
SYS_d7b1d3ee_AFE_AM3
1
2
SYS_fca12k5_AFEAGND
100n X7R 16V

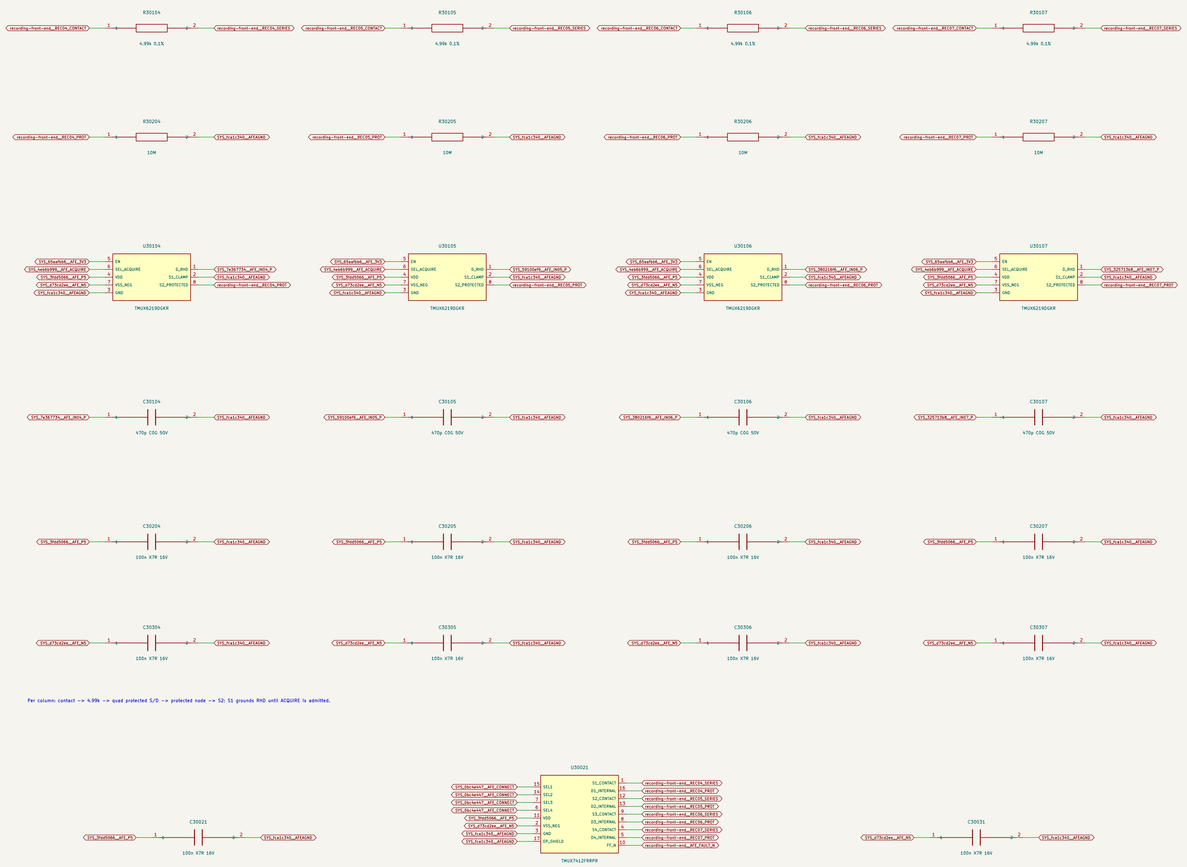
470pF is at the RHO pin; 10M bleeds the internal node. Switch capacitance/leakage/injection and shared-reference mismatch remain modeled assumptions.

Fault threshold follows +/-5V rails and is far outside RHO +/-0.4V linear DC range. External low-voltage qualification is mandatory before unclamping.

Native digital circuit slice; artificial signals only; external supervisors/power/PCB remain
Project SCCI RH
Sheet: /recording-front-end/bank0/
File: bank0.kicad_sch
Title: Project SCCI RH S4 / inputs 00-03 / protected recording
Size: A1 | Date: 2026-10-13 | **Rev: 0.1**
KiCad E.D.A. 10.0.6 | Id: 13/80

DIGITAL RESEARCH CIRCUIT / ARTIFICIAL SIGNALS / NO PCB OR IMPLANT QUALIFICATION

Spinal concept: 16 positive contacts + 1 shared reference + separate passive bias; amplifier linearity and biological recording remain conditional.



Per column: contact -> 4.99k -> quad protected S/D -> protected node -> S2; S1 grounds RHO until ACQUIRE is admitted.

470pF is at the RHO pin; 10M bleeds the internal node. Switch capacitance/leakage/injection and shared-reference mismatch remain modeled assumptions.

Fault threshold follows +/-5V rails and is far outside RHO +/-0.4V linear DC range. External low-voltage qualification is mandatory before unclamping.

Native digital circuit slice; artificial signals only; external supervisors/power/PCB remain

Project SCCI RH

Sheet: /recording-front-end/bank1/

File: bank1.kicad_sch

Title: Project SCCI RH S4 / inputs 04–07 / protected recording

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 14/80

DIGITAL RESEARCH CIRCUIT / ARTIFICIAL SIGNALS / NO PCB OR IMPLANT QUALIFICATION

Spinal concept: 16 positive contacts + 1 shared reference + separate passive bias; amplifier linearity and biological recording remain conditional.

R30108

recording-front-end_RECOB_CONTACT

4.99k 0.1%

recording-front-end_RECOB_SERVE1

R30109

recording-front-end_RECOA_CONTACT

4.99k 0.1%

recording-front-end_RECOA_SERVE1

R30110

recording-front-end_RECO3_CONTACT

4.99k 0.1%

recording-front-end_RECO3_SERVE1

R30111

recording-front-end_RECO2_CONTACT

4.99k 0.1%

recording-front-end_RECO2_SERVE1

R30208

recording-front-end_RECOB_PROT

10M

SYS_fca1c7e3_AFEAGND

R30209

recording-front-end_RECOA_PROT

10M

SYS_fca1c7e3_AFEAGND

R30210

recording-front-end_RECO3_PROT

10M

SYS_fca1c7e3_AFEAGND

R30211

recording-front-end_RECO2_PROT

10M

SYS_fca1c7e3_AFEAGND

U30108

SYS_65aef6b6_AFE_RDY

SYS_4e6b5999_AFE_ACQUIRE

SYS_9da05066_AFE_PS

SYS_d7bc2dee_AFE_AD

SYS_fca1c7e3_AFEAGND

EN

SEL_ACQUIRE

VDD

VSS_NEG

GND

RHD

S1_CLAMP

S2_PROTECTED

SYS_1dc2e43b_AFE_INJB_P

SYS_fca1c7e3_AFEAGND

recording-front-end_RECOB_PROT

TMUX6219DGKR

U30109

SYS_65aef6b6_AFE_RDY

SYS_4e6b5999_AFE_ACQUIRE

SYS_9da05066_AFE_PS

SYS_d7bc2dee_AFE_AD

SYS_fca1c7e3_AFEAGND

EN

SEL_ACQUIRE

VDD

VSS_NEG

GND

RHD

S1_CLAMP

S2_PROTECTED

SYS_ae792e88_AFE_INJA_P

SYS_fca1c7e3_AFEAGND

recording-front-end_RECOA_PROT

TMUX6219DGKR

U30110

SYS_65aef6b6_AFE_RDY

SYS_4e6b5999_AFE_ACQUIRE

SYS_9da05066_AFE_PS

SYS_d7bc2dee_AFE_AD

SYS_fca1c7e3_AFEAGND

EN

SEL_ACQUIRE

VDD

VSS_NEG

GND

RHD

S1_CLAMP

S2_PROTECTED

SYS_8b67c14a_AFE_INJ3_P

SYS_fca1c7e3_AFEAGND

recording-front-end_RECO3_PROT

TMUX6219DGKR

U30111

SYS_65aef6b6_AFE_RDY

SYS_4e6b5999_AFE_ACQUIRE

SYS_9da05066_AFE_PS

SYS_d7bc2dee_AFE_AD

SYS_fca1c7e3_AFEAGND

EN

SEL_ACQUIRE

VDD

VSS_NEG

GND

RHD

S1_CLAMP

S2_PROTECTED

SYS_b8a4cc85_AFE_INJ2_P

SYS_fca1c7e3_AFEAGND

recording-front-end_RECO2_PROT

TMUX6219DGKR

C30108

SYS_1dc2e43b_AFE_INJB_P

470p C0G 50V

SYS_fca1c7e3_AFEAGND

C30109

SYS_ae792e88_AFE_INJA_P

470p C0G 50V

SYS_fca1c7e3_AFEAGND

C30110

SYS_8b67c14a_AFE_INJ3_P

470p C0G 50V

SYS_fca1c7e3_AFEAGND

C30111

SYS_b8a4cc85_AFE_INJ2_P

470p C0G 50V

SYS_fca1c7e3_AFEAGND

C30208

SYS_9da05066_AFE_PS

100n X7R 16V

SYS_fca1c7e3_AFEAGND

C30209

SYS_9da05066_AFE_PS

100n X7R 16V

SYS_fca1c7e3_AFEAGND

C30210

SYS_9da05066_AFE_PS

100n X7R 16V

SYS_fca1c7e3_AFEAGND

C30211

SYS_9da05066_AFE_PS

100n X7R 16V

SYS_fca1c7e3_AFEAGND

C30308

SYS_d7bc2dee_AFE_AD

100n X7R 16V

SYS_fca1c7e3_AFEAGND

C30309

SYS_d7bc2dee_AFE_AD

100n X7R 16V

SYS_fca1c7e3_AFEAGND

C30310

SYS_d7bc2dee_AFE_AD

100n X7R 16V

SYS_fca1c7e3_AFEAGND

C30311

SYS_d7bc2dee_AFE_AD

100n X7R 16V

SYS_fca1c7e3_AFEAGND

Per column: contact -> 4.99k -> quad protected S/D -> protected node -> S2; S1 grounds RHD until ACQUIRE is admitted.

C30022

SYS_9da05066_AFE_PS

100n X7R 16V

SYS_fca1c7e3_AFEAGND

U30022

SYS_3bcbeeb7_AFE_CONNECT1

SYS_3bcbeeb7_AFE_CONNECT2

SYS_3bcbeeb7_AFE_CONNECT3

SYS_3bcbeeb7_AFE_CONNECT4

SYS_9da05066_AFE_PS

SYS_d7bc2dee_AFE_AD

SYS_fca1c7e3_AFEAGND

SEL1

SEL2

SEL3

SEL4

VDD

VSS_NEG

GND

EP_SHIELD

S1_CONTACT

S1_INTERNAL

S2_CONTACT

S2_INTERNAL

S3_CONTACT

S3_INTERNAL

S4_CONTACT

S4_INTERNAL

FF_A

recording-front-end_RECOB_SERVE

recording-front-end_RECOB_PROT

recording-front-end_RECOA_SERVE

recording-front-end_RECOA_PROT

recording-front-end_RECO3_SERVE

recording-front-end_RECO3_PROT

recording-front-end_RECO2_SERVE

recording-front-end_RECO2_PROT

recording-front-end_AFE_FAULT_A

TMUX7612FRRPR

C30032

SYS_d7bc2dee_AFE_AD

100n X7R 16V

SYS_fca1c7e3_AFEAGND

470pF is at the RHD pin; 10M bleeds the internal node. Switch capacitance/leakage/injection and shared reference mismatch remain modeled assumptions.

Fault threshold follows +/-5V rails and is far outside RHD +/-0.4V linear DC range. External low-voltage qualification is mandatory before unclamping.

Native digital circuit slice; artificial signals only; external supervisors/power/PCB remain

Project SCCI RH

Sheet: /recording-front-end/bank2/

File: bank2.kicad_sch

Title: Project SCCI RH S4 / inputs 08–11 / protected recording

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 15/80

DIGITAL RESEARCH CIRCUIT / ARTIFICIAL SIGNALS / NO PCB OR IMPLANT QUALIFICATION

Spinal concept: 16 positive contacts + 1 shared reference + separate passive bias; amplifier linearity and biological recording remain conditional.

R30112

recording-front-end_REC12_CONTACT

4.99k 0.1%

recording-front-end_REC12_SERIES

R30113

recording-front-end_REC13_CONTACT

4.99k 0.1%

recording-front-end_REC13_SERIES

R30114

recording-front-end_REC14_CONTACT

4.99k 0.1%

recording-front-end_REC14_SERIES

R30115

recording-front-end_REC15_CONTACT

4.99k 0.1%

recording-front-end_REC15_SERIES

R30212

recording-front-end_REC12_PROT

10M

SYS_fca1c7e5_AFEAGND

R30213

recording-front-end_REC13_PROT

10M

SYS_fca1c7e5_AFEAGND

R30214

recording-front-end_REC14_PROT

10M

SYS_fca1c7e5_AFEAGND

R30215

recording-front-end_REC15_PROT

10M

SYS_fca1c7e5_AFEAGND

U30112

SYS_65aef6b6_AFE_RST

SYS_4e6b5999_AFE_ACQUIRE

SYS_9da05066_AFE_PS

SYS_d7bc2dee_AFE_WR

SYS_fca1c7e5_AFEAGND

EN

SEL_ACQUIRE

VDD

VSS_NEG

GND

D_RHD

S1_CLAMP

S2_PROTECTED

SYS_49aeccc4_AFE_RCLP

SYS_fca1c7e5_AFEAGND

recording-front-end_REC12_PROT

TMUX8219DGKR

U30113

SYS_65aef6b6_AFE_RST

SYS_4e6b5999_AFE_ACQUIRE

SYS_9da05066_AFE_PS

SYS_d7bc2dee_AFE_WR

SYS_fca1c7e5_AFEAGND

EN

SEL_ACQUIRE

VDD

VSS_NEG

GND

D_RHD

S1_CLAMP

S2_PROTECTED

SYS_32c7e11c_AFE_RCLP

SYS_fca1c7e5_AFEAGND

recording-front-end_REC13_PROT

TMUX8219DGKR

U30114

SYS_65aef6b6_AFE_RST

SYS_4e6b5999_AFE_ACQUIRE

SYS_9da05066_AFE_PS

SYS_d7bc2dee_AFE_WR

SYS_fca1c7e5_AFEAGND

EN

SEL_ACQUIRE

VDD

VSS_NEG

GND

D_RHD

S1_CLAMP

S2_PROTECTED

SYS_4f1d5988_AFE_RCLP

SYS_fca1c7e5_AFEAGND

recording-front-end_REC14_PROT

TMUX8219DGKR

U30115

SYS_65aef6b6_AFE_RST

SYS_4e6b5999_AFE_ACQUIRE

SYS_9da05066_AFE_PS

SYS_d7bc2dee_AFE_WR

SYS_fca1c7e5_AFEAGND

EN

SEL_ACQUIRE

VDD

VSS_NEG

GND

D_RHD

S1_CLAMP

S2_PROTECTED

SYS_5321c999_AFE_RCLP

SYS_fca1c7e5_AFEAGND

recording-front-end_REC15_PROT

TMUX8219DGKR

C30112

SYS_49aeccc4_AFE_RCLP

470p C0G 50V

SYS_fca1c7e5_AFEAGND

C30113

SYS_32c7e11c_AFE_RCLP

470p C0G 50V

SYS_fca1c7e5_AFEAGND

C30114

SYS_4f1d5988_AFE_RCLP

470p C0G 50V

SYS_fca1c7e5_AFEAGND

C30115

SYS_5321c999_AFE_RCLP

470p C0G 50V

SYS_fca1c7e5_AFEAGND

C30212

SYS_9da05066_AFE_PS

100n X7R 16V

SYS_fca1c7e5_AFEAGND

C30213

SYS_9da05066_AFE_PS

100n X7R 16V

SYS_fca1c7e5_AFEAGND

C30214

SYS_9da05066_AFE_PS

100n X7R 16V

SYS_fca1c7e5_AFEAGND

C30215

SYS_9da05066_AFE_PS

100n X7R 16V

SYS_fca1c7e5_AFEAGND

C30312

SYS_d7bc2dee_AFE_WR

100n X7R 16V

SYS_fca1c7e5_AFEAGND

C30313

SYS_d7bc2dee_AFE_WR

100n X7R 16V

SYS_fca1c7e5_AFEAGND

C30314

SYS_d7bc2dee_AFE_WR

100n X7R 16V

SYS_fca1c7e5_AFEAGND

C30315

SYS_d7bc2dee_AFE_WR

100n X7R 16V

SYS_fca1c7e5_AFEAGND

Per column: contact -> 4.99k -> quad protected S/D -> protected node -> S2; S1 grounds RHD until ACQUIRE is admitted.

C30023

SYS_9da05066_AFE_PS

100n X7R 16V

SYS_fca1c7e5_AFEAGND

U30023

SYS_35c1e4a7_AFE_CONNECT

SYS_35c1e4a7_AFE_CONNECT

SYS_35c1e4a7_AFE_CONNECT

SYS_35c1e4a7_AFE_CONNECT

SYS_9da05066_AFE_PS

SYS_d7bc2dee_AFE_WR

SYS_fca1c7e5_AFEAGND

EP_SHIELD

SEL1

SEL2

SEL3

SEL4

VDD

VSS_NEG

GND

S1_CONTACT

S1_INTERNAL

S2_CONTACT

S2_INTERNAL

S3_CONTACT

S3_INTERNAL

S4_CONTACT

S4_INTERNAL

FF_A

recording-front-end_REC12_SERIES

recording-front-end_REC12_PROT

recording-front-end_REC13_SERIES

recording-front-end_REC13_PROT

recording-front-end_REC14_SERIES

recording-front-end_REC14_PROT

recording-front-end_REC15_SERIES

recording-front-end_REC15_PROT

recording-front-end_AFE_FAULT_N

TMUX7412FRWPR

C30033

SYS_d7bc2dee_AFE_WR

100n X7R 16V

SYS_fca1c7e5_AFEAGND

470pF is at the RHD pin; 10M bleeds the internal node. Switch capacitance/leakage/injection and shared-reference mismatch remain modeled assumptions.

Fault threshold follows +/-5V rails and is far outside RHD +/-0.4V linear DC range. External low-voltage qualification is mandatory before unclamping.

Native digital circuit slice; artificial signals only; external supervisors/power/PCB remain

Project SCCI RH

Sheet: /recording-front-end/bank3/

File: bank3.kicad_sch

Title: Project SCCI RH S4 / inputs 12–15 / protected recording

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 16/80

DIGITAL RESEARCH CIRCUIT / ARTIFICIAL SIGNALS / NO PCB OR IMPLANT QUALIFICATION

Spinal concept: 16 positive contacts + 1 shared reference + separate passive bias; amplifier linearity and biological recording remain conditional.

REF_CONTACT passes through the same disconnect/clamp topology; one AFE_REF node feeds all sixteen minus pins (192pF intrinsic typical).











BIAS_CONTACT is separate and never a stimulation return. Passive current arithmetic does not establish a medical current limit.













Native digital circuit slice; artificial signals only; external supervisors/power/PCB remain

Project SCCI RH

Sheet: /recording-front-end/reference/

File: reference.kicad_sch

Title: Project SCCI RH S4 / Shared reference / passive body bias

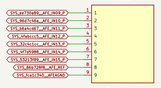
Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 17/80

INTEGRATED COMPONENT–TAP HARNESS / recording-front-end

Physical headers expose actual earlier component taps. Original connectors remain available.

Only named electrical nets connect. AFE, HOST and companion grounds remain distinct.



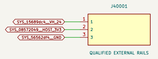


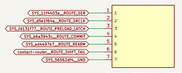
Artificial-load digital design. Added wiring capacitance and connector integrity require measurement.

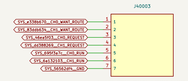
Project SCCI RH	
Sheet: /recording-front-end/integrated_component_taps/	
File: integration_taps.kicad_sch	
Title: Project SCCI RH / recording-front-end integration taps	
Size: A1 Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6	Id: 18/80

DIGITAL RESEARCH CIRCUIT / RESTRICTED 24 V, 3 mA SOURCES / ARTIFICIAL LOADS ONLY

Sixteen selectable stimulation contacts, two dedicated monitored returns; command-level routing is not measured continuity or isolation.

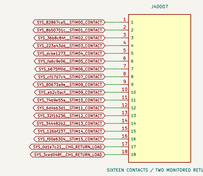












Required before COMMIT: both WANT/REQUEST/RUN low, independently observed quiescence, monitor permits, rails, recording isolation and watchdog valid.

Then: COMMIT -> read all eight active Q bits -> fresh verification ACK edge -> separate REARM -> assert route WANT -> allow settling before phase.

source0



File: source0.kicad_sch

source1



File: source1.kicad_sch

address



File: address.kicad_sch

admission



File: admission.kicad_sch

collision



File: collision.kicad_sch

No mux state sensor. Independent terminal cut-off, compliance detector, independent watchdog, rail generator. PCB or implanted device is completed here.

Native digital route slice; artificial loads; external protection/power/PCB remain

Project SCCI RH

Sheet: /contact-router/

File: contact_router.kicad_sch

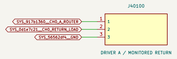
Title: Project SCCI RH S4 / Route interfaces and monitored returns

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 19/80

DIGITAL RESEARCH CIRCUIT / RESTRICTED 24 V, 3 mA SOURCES / ARTIFICIAL LOADS ONLY

Sixteen selectable stimulation contacts, two dedicated monitored returns; command-level routing is not measured continuity or isolation.

Both bank 0 commons share A_ROUTER_END = ROUTE_EN & MODE0; EN1 = ROUTE_EN & ADDR3. Addresses 000..111 select S1..S8.



















Dedicated return: external contact -> RETURN_LOAD -> existing monitor 2 ohm shunt -> RETURN_DRIVER -> current-driver B_BR.

Do not bypass the monitor, add a second shunt, tie the two returns, or use recording REF/BIAS as a stimulation return.

TMUX8208 is rail-to-rail at valid 24 V supply: powered-off, stuck-on, parasitic coupling and two-source shared tissue paths remain unqualified.

A_ROUTER needs external terminal guard qualification before connection to A_BR; internal enable-low is only a commanded off state.

Native digital route slice; artificial loads; external protection/power/PCB remain

Project SCCI RH

Sheet: /contact-router/source0/

File: source0.kicad_sch

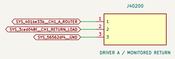
Title: Project SCCI RH S4 / Source 0 / sixteen-contact output

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 20/80

DIGITAL RESEARCH CIRCUIT / RESTRICTED 24 V, 3 mA SOURCES / ARTIFICIAL LOADS ONLY

Sixteen selectable stimulation contacts, two dedicated monitored returns; command-level routing is not measured continuity or isolation.

Both bank 0 commons share A_ROUTER_END = ROUTE_EN & MODE0; EN1 = ROUTE_EN & ADDR3. Addresses 000..111 select S1..S8.

























Dedicated return: external contact -> RETURN_LOAD -> existing monitor 2 ohm shunt -> RETURN_DRIVER -> current-driver B_BR.

Do not bypass the monitor, add a second shunt, tie the two returns, or use recording REF/BIAS as a stimulation return.

TMUX8208 is rail-to-rail at valid 24 V supply: powered-off, stuck-on, parasitic coupling and two-source shared tissue paths remain unqualified.

A_ROUTER needs external terminal guard qualification before connection to A_BR; internal enable-low is only a commanded off state.

Native digital route slice; artificial loads; external protection/power/PCB remain

Project SCCI RH

Sheet: /contact-router/source1/

File: source1.kicad_sch

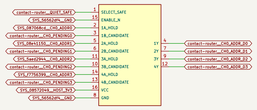
Title: Project SCCI RH S4 / Source 1 / sixteen-contact output

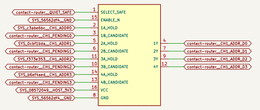
Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 21/80

DIGITAL RESEARCH CIRCUIT / RESTRICTED 24 V, 3 mA SOURCES / ARTIFICIAL LOADS ONLY

Sixteen selectable stimulation contacts, two dedicated monitored returns; command-level routing is not measured continuity or isolation.













Candidate bits may change without changing active addresses. Eight active flip-flops always see raw COMMIT clock; safe D selection loads or holds.

RESET_READY low asynchronously clears active bits to zero; outputs remain inhibited until legal COMMIT, fresh readback ACK and deliberate REARM.











































SRCLR affects only the candidate shift stage; QH_SHIFT is payload cascade, not active-address or analog switch readback. Actual Q bits appear at J6.

QUIET_SAFE and candidate data must meet physical setup/hold. Gate delay, asynchronous clear, metastability and clock-integrity qualification remain.

Native digital route slice; artificial loads; external protection/power/PCB remain

Project SCCI RH

Sheet: /contact-router/address/

File: address.kicad_sch

Title: Project SCCI RH S4 / Candidate preload and active addresses

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 22/80

DIGITAL RESEARCH CIRCUIT / RESTRICTED 24 V, 3 mA SOURCES / ARTIFICIAL LOADS ONLY

Sixteen selectable stimulation contacts, two dedicated monitored returns; command-level routing is not measured continuity or isolation.

BASE_HEALTH = RESET & RAILS & WATCHDOG & AFE_ISOLATED_READY & MONO & MON1; QUIET_SAFE additionally requires both WANT/REQUEST/RUN low and quiescence.

U40300

SYS_PFYbz58__RESET_READY

SYS_B3Yn79D7__RAILS_QUALIFIED

SYS_aKtnGr4u__WATCHDOG_OK

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G110DVR

contact-router__HEALTH_A

U40301

SYS_NK52J17k__AFE_ISOLATED_READY

SYS_5Bnbz13s__CH0_MON_PERMIT

SYS_ax51Lw8L__CH1_MON_PERMIT

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G110DVR

contact-router__HEALTH_B

U40302

contact-router__HEALTH_A

contact-router__HEALTH_B

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G08DBVR

contact-router__BASE_HEALTH

U40303

SYS_aT3Rb67S__CH1_WANT_ROUTE

SYS_B3nbb67s__CH1_WANT_ROUTE

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G32DBVR

contact-router__ANY_WANT

U40304

contact-router__ANY_WANT

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G04DBVR

contact-router__NO_WANT

U40305

SYS_aT3Rb67S__CH1_REQUEST

SYS_a6JN8269__CH1_REQUEST

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G32DBVR

contact-router__ANY_REQUEST

U40306

SYS_k9P57e7__CH1_RUN

SYS_Kte15J18__CH1_RUN

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G32DBVR

contact-router__ANY_RUN

U40307

contact-router__ANY_REQUEST

contact-router__ANY_RUN

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G32DBVR

contact-router__ANY_PHASE

U40308

contact-router__ANY_PHASE

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G04DBVR

contact-router__NO_PHASE

U40309

SYS_2q0eSbJx__CH1_QUIESCENT_OK

SYS_2Qeeab7J__CH1_QUIESCENT_OK

contact-router__BASE_HEALTH

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G110DVR

contact-router__QUIET_HEALTH

U40310

contact-router__NO_WANT

contact-router__NO_PHASE

contact-router__QUIET_HEALTH

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G11DBVR

contact-router__QUIET_SAFE

U40311

SYS_b6a39t7c__ROUTE_COMMIT

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G04DBVR

contact-router__COMMIT_A

U40312

contact-router__ROUTE_CONFLICT

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G04DBVR

contact-router__NO_CONFLICT

U40313

contact-router__BASE_HEALTH

contact-router__COMMIT_A

contact-router__NO_CONFLICT

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G110DBVR

contact-router__VALID_CLK_N

U40314

SYS_a6a7E57x__ROUTE_COMMIT

contact-router__QUIET_SAFE

contact-router__BASE_HEALTH

SYS_D8572Yn4__HOST_N29

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G74DCUR

contact-router__COMMIT_SEEN

U40315

contact-router__BASE_HEALTH

contact-router__COMMIT_A

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G08DBVR

contact-router__ACK_CLR_N

U40316

SYS_1Np7fGGL__ROUTE_ACTIVE_BITS_VERIFIED

contact-router__COMMIT_SEEN

contact-router__ACK_CLR_N

SYS_D8572Yn4__HOST_N29

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G74DCUR

contact-router__READBACK_SEEN

U40317

contact-router__COMMIT_SEEN

contact-router__QUIET_SAFE

contact-router__READBACK_SEEN

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G110DBVR

contact-router__REARM_A

U40318

SYS_ga4n57k7__ROUTE_REARM

contact-router__REARM_A

contact-router__VALID_CLK_N

SYS_D8572Yn4__HOST_N29

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G74DCUR

contact-router__ROUTE_VALID

U40319

contact-router__ROUTE_VALID

contact-router__BASE_HEALTH

contact-router__COMMIT_A

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G110DBVR

contact-router__READY_A

U40320

contact-router__READY_A

contact-router__NO_CONFLICT

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G08DBVR

SYS_6cCL2Q6s__ROUTE_COMMAND_READY

U40321

contact-router__ROUTE_VALID

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

SN74LVC1G04DBVR

contact-router__ROUTE_BLOCK

C40300

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

100n X7R 10V

C40301

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40302

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40303

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40304

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40305

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40306

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40307

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40308

SYS_56562zPL__GND

SYS_56562zPL__GND

100n X7R 10V

C40309

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

100n X7R 10V

C40310

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40311

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40312

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40313

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40314

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40315

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40316

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40317

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40318

SYS_D8572Yn4__HOST_N29

SYS_56562zPL__GND

100n X7R 10V

C40319

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40320

SYS_56562zPL__GND

SYS_D8572Yn4__HOST_N29

100n X7R 10V

C40321

SYS_56562zPL__GND

SYS_56562zPL__GND

100n X7R 10V

R40300

SYS_PFYbz58__RESET_READY

10k

R40301

SYS_B3Yn79D7__RAILS_QUALIFIED

10k

R40302

SYS_aKtnGr4u__WATCHDOG_OK

10k

R40303

SYS_NK52J17k__AFE_ISOLATED_READY

10k

R40304

SYS_2q0eSbJx__CH0_QUIESCENT_OK

10k

R40305

SYS_2Qeeab7J__CH1_QUIESCENT_OK

10k

R40306

SYS_1Np7fGGL__ROUTE_ACTIVE_BITS_VERIFIED

10k

R40307

SYS_5Bnbz13s__CH0_MON_PERMIT

10k

R40308

SYS_ax51Lw8L__CH1_MON_PERMIT

10k

R40309

SYS_aT3Rb67S__CH1_WANT_ROUTE

10k

R40310

SYS_aT3Rb67S__CH1_REQUEST

10k

R40311

SYS_aT3Rb67S__CH1_RUN

10k

R40312

SYS_k9P57e7__CH1_RUN

10k

R40313

SYS_56562zPL__GND

10k

R40314

SYS_56562zPL__GND

10k

Any COMMIT invalidates prior validation and ACK. Illegal COMMIT holds active bits and captures COMMIT_SEEN=0.

Rearm needs a fresh post-commit ACK edge. Health recovery or collision removal cannot create a clock edge or restart output.

Ideal logic only: setup/hold, all-off settling, voltage, independent watchdog and actual current observation remain mandatory.

Native digital route slice; artificial loads; external protection/power/PCB remain

Project SCCI RH

Sheet: /contact-router/admission/

File: admission.kicad_sch

Title: Project SCCI RH S4 / Commit, acknowledgement and rearm

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 23/80

DIGITAL RESEARCH CIRCUIT / RESTRICTED 24 V, 3 mA SOURCES / ARTIFICIAL LOADS ONLY

Sixteen selectable stimulation contacts, two dedicated monitored returns; command-level routing is not measured continuity or isolation.

Conflict = WANT0 & WANT1 & equal(all four active address bits). It disables BOTH bank families and asynchronously clears route validation.

U40400

SN74LVC1G86DBVR

U40401

SN74LVC1G86DBVR

U40402

SN74LVC1G86DBVR

U40403

SN74LVC1G86DBVR

U40404

SN74LVC1G32DBVR

U40405

SN74LVC1G32DBVR

U40406

SN74LVC1G32DBVR

U40407

SN74LVC1G04DBVR

U40408

SN74LVC1G11DBVR

U40409

SN74LVC1G08DBVR

U40410

SN74LVC1G04DBVR

U40411

SN74LVC1G08DBVR

U40412

SN74LVC1G08DBVR

U40413

SN74LVC1G08DBVR

U40414

SN74LVC1G08DBVR

U40415

SN74LVC1G04DBVR

U40416

SN74LVC1G08DBVR

U40417

SN74LVC1G08DBVR

U40418

SN74LVC1G08DBVR

C40400

100n X7R 10V

C40401

100n X7R 10V

C40402

100n X7R 10V

C40403

100n X7R 10V

C40404

100n X7R 10V

C40405

100n X7R 10V

C40406

100n X7R 10V

C40407

100n X7R 10V

C40408

100n X7R 10V

C40409

100n X7R 10V

C40410

100n X7R 10V

C40411

100n X7R 10V

C40412

100n X7R 10V

C40413

100n X7R 10V

C40414

100n X7R 10V

C40415

100n X7R 10V

C40416

100n X7R 10V

C40417

100n X7R 10V

C40418

100n X7R 10V

Removing a conflict only removes its fault condition: it does not restore VALID. Release both WANTs, verify quiet, then explicitly rearm.

The two source enables may coexist only at different contacts. Common tissue impedance and volume conduction are outside this digital collision test.

ROUTE_LOCKED means admitted digital command ownership only. No selected-contact continuity or power-off isolation is inferred.

Native digital route slice; artificial loads; external protection/power/PCB remain

Project SCCI RH

Sheet: /contact-router/collision/

File: collision.kicad_sch

Title: Project SCCI RH S4 / Conflict and bank enables

Size: A1	Date: 2026-10-13	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 24/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHO-side windows; conditional healthy-switch blanking is not proven isolation.

J50001

- SYS_a4932174__SIGP_3V3
- SYS_48eeaf9b__SIGP_A
- SYS_88572240__HOST_3V3
- SYS_ce104858__HOST_A
- SYS_fb223756__GN_S3
- SYS_1f68f6ca__GN_S5
- SYS_56562294__GND

EXTERNAL SUPERVISOR AND HOST RAILS

J50002

- SYS_f3ee9b56__AFE_3V3
- SYS_39d5056d__AFE_5V
- SYS_af7b1d4e__AFE_A5
- SYS_7ce17e6_AFEAGND
- SYS_54c1ee7c__AFE_CONNECT
- SYS_ea66b998__AFE_ACQUIRE

FLOATING AFE RAILS AND OBSERVED CONTROLS

J50003

- SYS_65555e6e__SIGP_REARM
- SYS_82553898__FAULT_RESET
- SYS_29baee1c_WD
- SYS_48e45f03__CHA_REQUEST
- SYS_ed288265__CH1_REQUEST
- SYS_69f0267c__CHA_MUX
- SYS_6e132101__CH1_MUX
- SYS_1f47477a__CH1_ROUTE_LOCKED
- SYS_8429f705__CH1_ROUTE_LOCKED
- SYS_7d48be1c_PHASE_REARM
- SYS_48e29157__PHASE_REARM
- SYS_5b562d9c__GND

RAW CONTROL / STATUS

J50004

- SYS_9be39273__CHA1_MODE
- SYS_5bbd4a4c__CH1_A_MODE
- SYS_57b982ba__MODE_SHED
- SYS_48827126__MODE_HOST
- SYS_58ebc231__CHA_MODE_PERMIT
- SYS_ce7312eb__CH1_MODE_PERMIT
- SYS_49ee119a__CH1_EXT_SIGP_3V3
- SYS_bbfa894a__CH1_EXT_SIGP_5V
- SYS_56562294__GND

EXISTING MONITOR OBSERVATIONS

J50005

- SYS_4f7bb7dc__AFE1ET_MEAS
- SYS_93b17b57__Bell1_SinePlt
- SYS_a83d49fc__WATCHDOG_OK
- SYS_8d5217e__AFE_OSCILATE_MEAS
- SYS_2b9e5b2e__CH1_QUIESCENT_OK
- SYS_20bbe6c1__CH1_QUIESCENT_OK
- SYS_e3b7c7fe__CH1_EXT_SIGP_OK
- SYS_8f0f04ce__CH1_EXT_SIGP_OK
- SYS_98c55081__SIGP_ARMED
- supervision__CH1_ACQ
- supervision__CH1_ACQ_OK
- SYS_7fc27e0d__GLOBAL_QUARD_OK
- SYS_56562294__GND

EXPORTED NATIVE HEALTH / PERMISSION

J50006

- SYS_8175176b__CH1_A_ROUTE
- SYS_ee176f57__CH1_A_OK
- SYS_c651ee7b__CH1_A_ROUTE
- SYS_c7314b6c__CH1_A_OK
- SYS_56562294__GND

DRIVER INTERNAL DIFFERENTIAL VOLTAGES

SYS_a4932174__SIGP_3V3

SYS_48eeaf9b__SIGP_A

guards

File: guards.kicad_sch

afe_rails

File: afe_rails.kicad_sch

quiescence

File: quiescence.kicad_sch

admission

File: admission.kicad_sch

phase1

File: phase1.kicad_sch

afe_bank2

File: afe_bank2.kicad_sch

afe_logic

File: afe_logic.kicad_sch

host_rails

File: host_rails.kicad_sch

afe_rails_2

File: afe_rails_2.kicad_sch

voltage

File: voltage.kicad_sch

admission_2

File: admission_2.kicad_sch

afe_bank0

File: afe_bank0.kicad_sch

afe_bank3

File: afe_bank3.kicad_sch

afe_logic_2

File: afe_logic_2.kicad_sch

host_rails_2

File: host_rails_2.kicad_sch

watchdog

File: watchdog.kicad_sch

duration

File: duration.kicad_sch

phase0

File: phase0.kicad_sch

afe_bank1

File: afe_bank1.kicad_sch

afe_bank4

File: afe_bank4.kicad_sch

defaults

File: defaults.kicad_sch

integrated_component_taps

File: integration_taps.kicad_sch

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/

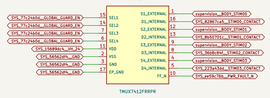
File: supervision.kicad_sch

Title: Project SCCI RH S4 / Interfaces and handoff

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 25/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHO-side windows; conditional healthy-switch blanking is not proven isolation.









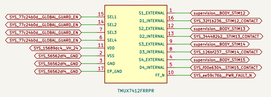












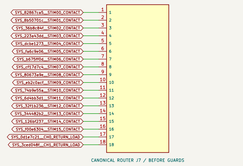


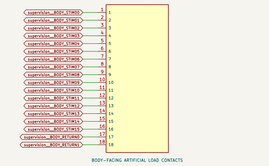














All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/guards/

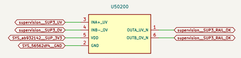
File: guards.kicad_sch

Title: Project SCCI RH S4 / 18 body-side terminal guards

Size: A1 Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6	Id: 26/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.





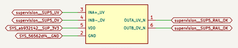








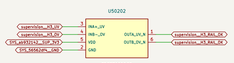
























All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/host_rails/

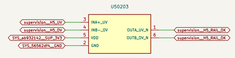
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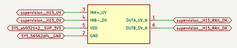
Title: Project SCCI RH S4 / Host supply windows

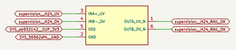
Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 27/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.









All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/host_rails_2/

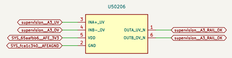
File: host_rails_2.kicad_sch

Title: Project SCCI RH S4 / Host supply windows / 2

Size: A1 Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6	Id: 28/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.





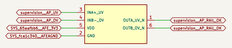














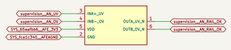














All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/afe_rails/

File: afe_rails.kicad_sch

Title: Project SCCI RH S4 / AFE supply windows

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 29/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.





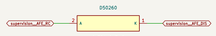


















All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/afe_rails_2/

File: afe_rails_2.kicad_sch

Title: Project SCCI RH S4 / AFE supply windows / 2

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 30/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHO-side windows; conditional healthy-switch blanking is not proven isolation.

R50250
100k 1%
SYS_ads9327s2__SIGP_SCK
supervision__SIGP_SCK

C50250
47n X7R 10%
supervision__SIGP_SCK
SYS_5050249%__GND

D50250
BAT54WS-7-F
supervision__SIGP_SCK
supervision__SIGP_SDI

R50251
100R
supervision__SIGP_SDI
SYS_ads9327s2__SIGP_SDI

U50250
SN74LVC1G17DBVR
supervision__SIGP_SCK
SYS_ads9327s2__SIGP_SDI
SYS_5050249%__GND
supervision__SIGP_STARTUP_CH

C50251
100n X7R 16V
SYS_ads9327s2__SIGP_SDI
SYS_5050249%__GND

U51000
SN74LVC1G1108VR
supervision__SIGP3_ENCL_CK
supervision__SIGP3_ENCL_CH
supervision__HS_ENCL_CH
SYS_ads9327s2__SIGP_SDI
SYS_5050249%__GND
supervision__HOST_ENCL_CH_ST

C51000
100n X7R 16V
SYS_ads9327s2__SIGP_SDI
SYS_5050249%__GND

U51001
SN74LVC1G1108VR
supervision__HOST_ENCL_CK_ST
supervision__HS_ENCL_CK
supervision__ECG_ENCL_CK
SYS_ads9327s2__SIGP_SDI
SYS_5050249%__GND
supervision__HOST_ENCL_CK_LS

C51001
100n X7R 16V
SYS_ads9327s2__SIGP_SDI
SYS_5050249%__GND

U51002
SN74LVC1G1108VR
supervision__HOST_ENCL_CK_LS
supervision__ACS_ENCL_CK
supervision__SIP_STARTUP_CH
SYS_ads9327s2__SIGP_SDI
SYS_5050249%__GND
supervision__HOST_ENCL_CK

C51002
100n X7R 16V
SYS_ads9327s2__SIGP_SDI
SYS_5050249%__GND

U50300
TPS2531DRBR
SYS_ads9327s1__SIGP_SDI
supervision__WDI_CWD
supervision__HOST_ENCL_CK
SYS_5050249%__GND
SYS_ePowerS__WDI
SYS_5050249%__GND
WDO_FAILING
CP_GND
WDO_B
ENOUT
supervision__WDI_ENOUT_CH
supervision__WDI_ENOUT_CH

R50300
10k
SYS_ads9327s2__SIGP_SCK
supervision__WDI_CWD

R50301
10k
SYS_ads9327s2__SIGP_SCK
supervision__WDI_ENOUT_CH

R50302
10k
SYS_ePowerS__WDI
SYS_5050249%__GND

C50300
100n X7R 16V
SYS_ads9327s2__SIGP_SCK
SYS_5050249%__GND

U51005
SN74LVC1G04DBVR
SYS_ePowerS__WDI
SYS_ads9327s1__SIGP_SCK
SYS_5050249%__GND
supervision__WDI_N

C51005
100n X7R 16V
SYS_ads9327s2__SIGP_SCK
SYS_5050249%__GND

U51006
SN74LVC1G08DBVR
supervision__WDI_ENOUT_CH
supervision__HOST_ENCL_CH
SYS_ads9327s1__SIGP_SCK
SYS_5050249%__GND
supervision__WDI_SEEN_CLR_N

C51006
100n X7R 16V
SYS_ads9327s2__SIGP_SCK
SYS_5050249%__GND

U50301
SN74LVC1G74DCUR
supervision__WDI_N
supervision__WDI_ENOUT_CH
supervision__WDI_SEEN_CLR_N
SYS_ads9327s2__SIGP_SCK
SYS_ads9327s1__SIGP_SCK
SYS_5050249%__GND
supervision__WDI_SEEN

C50301
100n X7R 16V
SYS_ads9327s2__SIGP_SCK
SYS_5050249%__GND

U51007
SN74LVC1G1108VR
supervision__WDI_ENOUT_CH
supervision__WDI_SEEN
supervision__HOST_ENCL_CH
SYS_ads9327s1__SIGP_SCK
SYS_5050249%__GND
supervision__WDI_GOOD

C51007
100n X7R 16V
SYS_ads9327s2__SIGP_SCK
SYS_5050249%__GND

U51008
SN74LVC1G08DBVR
supervision__WDI_GOOD
SYS_ads9327s2__SIGP_SCK
SYS_ads9327s1__SIGP_SCK
SYS_5050249%__GND
SYS_ab5044hs__WATCHDOG_OK

C51008
100n X7R 16V
SYS_ads9327s2__SIGP_SCK
SYS_5050249%__GND

All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain
Project SCCI RH
Sheet: /supervision/watchdog/
File: watchdog.kicad_sch

Title: Project SCCI RH S4 / Heartbeat and startup

Size: A1	Date: 2026-10-14
KiCad E.D.A. 10.0.6	**Rev: 0.1**
	Id: 31/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.





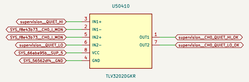




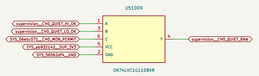










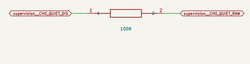






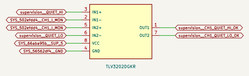




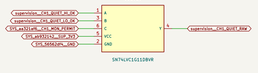


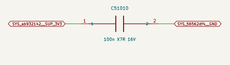
























All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/quiescence/

File: quiescence.kicad_sch

Title: Project SCCI RH S4 / Current quiet window

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 32/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHO-side windows; conditional healthy-switch blanking is not proven isolation.

R50500

SYS_VA50515__MON_VREF

252k 0.1%

supervision__PWR_HI_DIV

R50501

supervision__PWR_HI_DIV

536k 0.1%

supervision__PWR_LO_DIV

R50502

supervision__PWR_LO_DIV

252k 0.1%

SYS_50562#PL__GND

U50500

OPA391DCKR

supervision__PWR_HI_DIV

supervision__PWR_HI

SYS_66eaa90b__SUP_5

SYS_50562#PL__GND

supervision__PWR_HI

C50500

SYS_66eaa90b__SUP_5

100n X7R 16V

SYS_50562#PL__GND

U50501

OPA391DCKR

supervision__PWR_LO_DIV

supervision__PWR_LO

SYS_66eaa90b__SUP_5

SYS_50562#PL__GND

supervision__PWR_LO

C50501

SYS_66eaa90b__SUP_5

100n X7R 16V

SYS_50562#PL__GND

U50502

OPA2192IDGKR

supervision__CH1_DIFF_P

supervision__CH1_DIFF_N

supervision__CH2_DIFF_P

supervision__CH2_DIFF_N

SYS_66eaa90b__SUP_5

SYS_50562#PL__GND

SYS_1e9f8dd5__CH1_VPROB

SYS_42eeaa3c__CH1_VPROB

C50502

SYS_66eaa90b__SUP_5

100n X7R 16V

SYS_50562#PL__GND

R50510

SYS_617b1765__CH2_A_RSOTER

1M 0.1%

supervision__CH2_DIFF_P

R50511

SYS_57c4d2a__MON_VMID

49.9k 0.1%

supervision__CH1_DIFF_P

R50512

SYS_ee47bf53__CH1_B_BR

1M 0.1%

supervision__CH1_DIFF_N

R50513

SYS_1e9f8dd5__CH1_VPROB

49.9k 0.1%

supervision__CH1_DIFF_N

U50510

TLV320ZDGKR

supervision__PWR_HI

SYS_1e9f8dd5__CH1_VPROB

SYS_1e9f8dd5__CH1_VPROB

supervision__PWR_LO

SYS_66eaa90b__SUP_5

SYS_50562#PL__GND

supervision__CH1_PWR_HI_DIV

supervision__CH1_PWR_LO_DIV

C50510

SYS_66eaa90b__SUP_5

100n X7R 16V

SYS_50562#PL__GND

U51011

SN74LVC1G08DBVR

supervision__CH2_PWR_HI_DIV

supervision__CH2_PWR_LO_DIV

SYS_ab932174__SUP_3V3

SYS_50562#PL__GND

supervision__CH2_PWR_HI

C51011

SYS_ab932174__SUP_3V3

100n X7R 16V

SYS_50562#PL__GND

R50520

SYS_45116e37b__CH1_A_RSOTER

1M 0.1%

supervision__CH1_DIFF_P

R50521

SYS_57c4d2a__MON_VMID

49.9k 0.1%

supervision__CH1_DIFF_P

R50522

SYS_7f1180be__CH1_B_BR

1M 0.1%

supervision__CH1_DIFF_N

R50523

SYS_42eeaa3c__CH1_VPROB

49.9k 0.1%

supervision__CH1_DIFF_N

U50520

TLV320ZDGKR

supervision__PWR_HI

SYS_42eeaa3c__CH1_VPROB

supervision__PWR_LO

SYS_66eaa90b__SUP_5

SYS_50562#PL__GND

supervision__CH1_PWR_HI_DIV

supervision__CH1_PWR_LO_DIV

C50520

SYS_66eaa90b__SUP_5

100n X7R 16V

SYS_50562#PL__GND

U51012

SN74LVC1G08DBVR

supervision__CH1_PWR_HI_DIV

supervision__CH1_PWR_LO_DIV

SYS_ab932174__SUP_3V3

SYS_50562#PL__GND

supervision__CH1_PWR_LO

C51012

SYS_ab932174__SUP_3V3

100n X7R 16V

SYS_50562#PL__GND

All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/voltage/

File: voltage.kicad_sch

Title: Project SCCI RH S4 / Differential compliance

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 33/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.























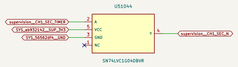








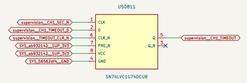














All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/duration/

File: duration.kicad_sch

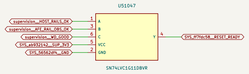
Title: Project SCCI RH S4 / Secondary phase duration

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 34/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

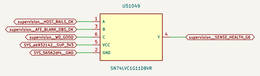
18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.

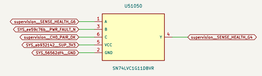












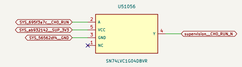




















All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/admission/

File: admission.kicad_sch

Title: Project SCCI RH S4 / Sticky permission and rearm

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 35/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHO-side windows; conditional healthy-switch blanking is not proven isolation.





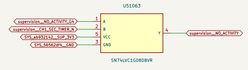




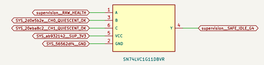


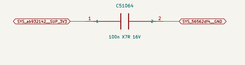






















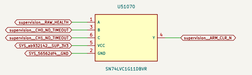






















All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/admission_2/

File: admission_2.kicad_sch

Title: Project SCCI RH S4 / Sticky permission and rearm / 2

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 36/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHO-side windows; conditional healthy-switch blanking is not proven isolation.

U51071



SN74LVC1G110BVR

C51071



U51072



SN74LVC1G08DBVR

C51072



U51073



SN74LVC1G04DBVR

C51073



U51074



SN74LVC1G08DBVR

C51074



U51075



SN74LVC1G11DBVR

C51075



U51076



SN74LVC1G11DBVR

C51076



U51077

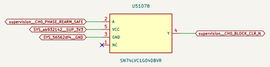


SN74LVC1G08DBVR

C51077



U51078

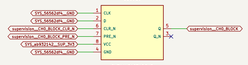


SN74LVC1G04DBVR

C51078



U50910

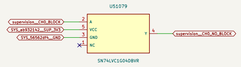


SN74LVC1G74DCUR

C50910



U51079



SN74LVC1G04DBVR

C51079



U51080



SN74LVC1G11DBVR

C51080



U51081



SN74LVC1G11DBVR

C51081



U51082

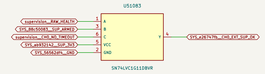


SN74LVC1G08DBVR

C51082



U51083



SN74LVC1G11DBVR

C51083



All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/phase0/

File: phase0.kicad_sch

Title: Project SCCI RH S4 / Source 0 phase permission

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 37/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHO-side windows; conditional healthy-switch blanking is not proven isolation.











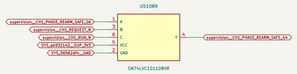






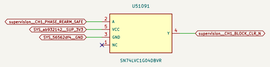






































All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/phase1/

File: phase1.kicad_sch

Title: Project SCCI RH S4 / Source 1 phase permission

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 38/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.

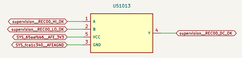




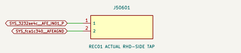














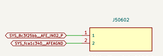










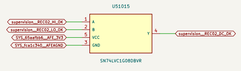


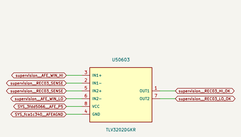
























All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/afe_bank0/

File: afe_bank0.kicad_sch

Title: Project SCCI RH S4 / RHD input windows 0

Size: A1 Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6	Id: 39/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.

J50604

SYS_%7677754__AFE_HAEN_P

SYS_tra1c7e3__AFEAGND

RECO4 ACTUAL RHD-SIDE TAP

R56040

SYS_%7677754__AFE_HAEN_P

10M 0.1%

supervision__RECO5_SENSE

R56041

SYS_85ae9bb6__AFE_IN5

1M 0.1%

supervision__RECO5_SENSE

U50604

supervision__AFE_WIN_HI

supervision__RECO5_SENSE

supervision__RECO4_SENSE

supervision__AFE_WIN_LO

SYS_9da05b6d__AFE_IP5

SYS_tra1c7e3__AFEAGND

IN1+

IN1−

IN2+

IN2−

VCC

GND

OUT1

OUT2

supervision__RECO5_HI_OK

supervision__RECO5_LO_OK

TLV320204AR

C50604

SYS_9da05b6d__AFE_IP5

100n X7R 16V

SYS_tra1c7e3__AFEAGND

U51017

supervision__RECO5_HI_OK

supervision__RECO5_LO_OK

SYS_85ae9bb6__AFE_IN5

SYS_tra1c7e3__AFEAGND

A

B

VCC

GND

Y

supervision__RECO5_DF_OK

SN74LVC1G08DBVR

C51017

SYS_85ae9bb6__AFE_IN5

100n X7R 16V

SYS_tra1c7e3__AFEAGND

J50605

SYS_69150ef4__AFE_HAEN_P

SYS_tra1c7e3__AFEAGND

RECO5 ACTUAL RHD-SIDE TAP

R56050

SYS_69150ef4__AFE_HAEN_P

10M 0.1%

supervision__RECO5_SENSE

R56051

SYS_85ae9bb6__AFE_IN5

1M 0.1%

supervision__RECO5_SENSE

U50605

supervision__AFE_WIN_HI

supervision__RECO5_SENSE

supervision__RECO6_SENSE

supervision__AFE_WIN_LO

SYS_9da05b6d__AFE_IP5

SYS_tra1c7e3__AFEAGND

IN1+

IN1−

IN2+

IN2−

VCC

GND

OUT1

OUT2

supervision__RECO5_HI_OK

supervision__RECO5_LO_OK

TLV320204AR

C50605

SYS_9da05b6d__AFE_IP5

100n X7R 16V

SYS_tra1c7e3__AFEAGND

U51018

supervision__RECO5_HI_OK

supervision__RECO5_LO_OK

SYS_85ae9bb6__AFE_IN5

SYS_tra1c7e3__AFEAGND

A

B

VCC

GND

Y

supervision__RECO5_DF_OK

SN74LVC1G08DBVR

C51018

SYS_85ae9bb6__AFE_IN5

100n X7R 16V

SYS_tra1c7e3__AFEAGND

J50606

SYS_%8211d4__AFE_HAEN_P

SYS_tra1c7e3__AFEAGND

RECO6 ACTUAL RHD-SIDE TAP

R56060

SYS_%8211d4__AFE_HAEN_P

10M 0.1%

supervision__RECO6_SENSE

R56061

SYS_85ae9bb6__AFE_IN5

1M 0.1%

supervision__RECO6_SENSE

U50606

supervision__AFE_WIN_HI

supervision__RECO6_SENSE

supervision__RECO6_SENSE

supervision__AFE_WIN_LO

SYS_9da05b6d__AFE_IP5

SYS_tra1c7e3__AFEAGND

IN1+

IN1−

IN2+

IN2−

VCC

GND

OUT1

OUT2

supervision__RECO6_HI_OK

supervision__RECO6_LO_OK

TLV320204AR

C50606

SYS_9da05b6d__AFE_IP5

100n X7R 16V

SYS_tra1c7e3__AFEAGND

U51019

supervision__RECO6_HI_OK

supervision__RECO6_LO_OK

SYS_85ae9bb6__AFE_IN5

SYS_tra1c7e3__AFEAGND

A

B

VCC

GND

Y

supervision__RECO6_DF_OK

SN74LVC1G08DBVR

C51019

SYS_85ae9bb6__AFE_IN5

100n X7R 16V

SYS_tra1c7e3__AFEAGND

J50607

SYS_32017b56__AFE_HAEF_P

SYS_tra1c7e3__AFEAGND

RECO7 ACTUAL RHD-SIDE TAP

R56070

SYS_32017b56__AFE_HAEF_P

10M 0.1%

supervision__RECO7_SENSE

R56071

SYS_85ae9bb6__AFE_IN5

1M 0.1%

supervision__RECO7_SENSE

U50607

supervision__AFE_WIN_HI

supervision__RECO7_SENSE

supervision__RECO7_SENSE

supervision__AFE_WIN_LO

SYS_9da05b6d__AFE_IP5

SYS_tra1c7e3__AFEAGND

IN1+

IN1−

IN2+

IN2−

VCC

GND

OUT1

OUT2

supervision__RECO7_HI_OK

supervision__RECO7_LO_OK

TLV320204AR

C50607

SYS_9da05b6d__AFE_IP5

100n X7R 16V

SYS_tra1c7e3__AFEAGND

U51020

supervision__RECO7_HI_OK

supervision__RECO7_LO_OK

SYS_85ae9bb6__AFE_IN5

SYS_tra1c7e3__AFEAGND

A

B

VCC

GND

Y

supervision__RECO7_DF_OK

SN74LVC1G08DBVR

C51020

SYS_85ae9bb6__AFE_IN5

100n X7R 16V

SYS_tra1c7e3__AFEAGND

All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/afe_bank1/

File: afe_bank1.kicad_sch

Title: Project SCCI RH S4 / RHD input windows 1

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 40/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.





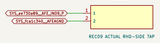














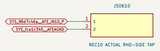












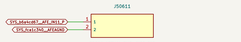






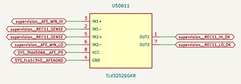


















All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/afe_bank2/

File: afe_bank2.kicad_sch

Title: Project SCCI RH S4 / RHD input windows 2

Size: A1 Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6	Id: 41/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.

J50612
REC12 ACTUAL RHD-SIDE TAP

R56120
10M 0.1%

R56121
1M 0.1%

U50612
TLV320204GKR

C50612
100n X7R 16V

U51025
SN74LVC1G08DBVR

C51025
100n X7R 16V

J50613
REC13 ACTUAL RHD-SIDE TAP

R56130
10M 0.1%

R56131
1M 0.1%

U50613
TLV320204GKR

C50613
100n X7R 16V

U51026
SN74LVC1G08DBVR

C51026
100n X7R 16V

J50614
REC14 ACTUAL RHD-SIDE TAP

R56140
10M 0.1%

R56141
1M 0.1%

U50614
TLV320204GKR

C50614
100n X7R 16V

U51027
SN74LVC1G08DBVR

C51027
100n X7R 16V

J50615
REC15 ACTUAL RHD-SIDE TAP

R56150
10M 0.1%

R56151
1M 0.1%

U50615
TLV320204GKR

C50615
100n X7R 16V

U51028
SN74LVC1G08DBVR

C51028
100n X7R 16V

All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/afe_bank3/

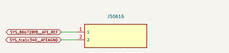
File: afe_bank3.kicad_sch

Title: Project SCCI RH S4 / RHD input windows 3

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 42/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.















All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/afe_bank4/

File: afe_bank4.kicad_sch

Title: Project SCCI RH S4 / RHD input windows 4

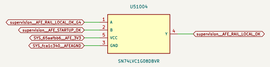
Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 43/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors. 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.







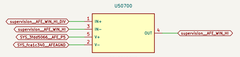




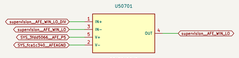




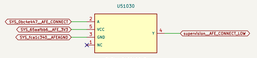




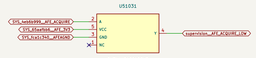






















All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/afe_logic/

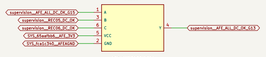
File: afe_logic.kicad_sch

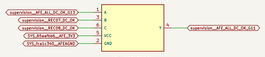
Title: Project SCCI RH S4 / AFE blank and isolated status

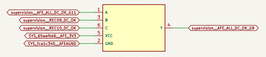
Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 44/80

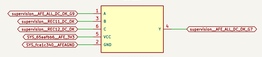
DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

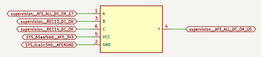
18 guarded stimulation conductors. 17 measured RHO-side windows; conditional healthy-switch blanking is not proven isolation.





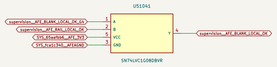


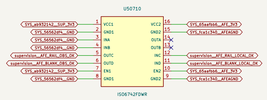












All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/afe_logic_2/

File: afe_logic_2.kicad_sch

Title: Project SCCI RH S4 / AFE blank and isolated status / 2

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 45/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / NATIVE INDEPENDENT SUPERVISION

18 guarded stimulation conductors, 17 measured RHD-side windows; conditional healthy-switch blanking is not proven isolation.

























All net labels are native electrical connections. Actual physical delay, leakage, failed switches and shared supplies remain bounded limitations.

Independent phase cap, heartbeat watchdog, rail windows and deliberate rearm have different functions. No automatic retry or reverse pulse.

Native supervision: converters, firmware, PCB and implant qualification remain

Project SCCI RH

Sheet: /supervision/defaults/

File: defaults.kicad_sch

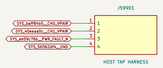
Title: Project SCCI RH S4 / External defaults

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 46/80

INTEGRATED COMPONENT—TAP HARNESS / supervision

Physical headers expose actual earlier component taps. Original connectors remain available.

Only named electrical nets connect. AFE, HOST and companion grounds remain distinct.



Artificial-load digital design. Added wiring capacitance and connector integrity require measurement.

Project SCCI RH
Sheet: /supervision/integrated_component_taps/
File: integration_taps.kicad_sch
Title: Project SCCI RH / supervision integration taps
Size: A1 Date: 2026-10-14 Rev: 0.1
KiCad E.D.A. 10.0.6 Id: 47/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.

J60001

power__PACK_POS

SYS_SENSE2P4__GND

ATJ1004 PROTECTED 25 PACK / 6A TO 8.4V

J60002

power__PWR_REQUEST

power__SUP_READY

power__BATT_OK

power__HOST_ENABLE

power__BOOST_ENABLE

power__HOST_RAIL_PG

power__HOST_V_PG

power__SUP_RAIL_PG

power__SUP_V_PG

SYS_unSIG1742__SUP_RST

SYS_enSIG750__PWR_FAULT_N

SYS_SENSE2P4__GND

POWER REQUEST / STATUS

J60003

SYS_unSIG1742__SUP_RST

SYS_dVdetPOL__SUP_V

SYS_SMT32H7A__HOST_RST

SYS_unLOADSW__HOST_V

SYS_R3237TR__VA_EN

SYS_LTC6804x1__VA_EN

SYS_SENSE2P4__GND

HOST AND SUPERVISOR RAILS

J60004

SYS_dVdetNeN__AFE_RST

SYS_TestCON4__AFE_EN

SYS_nTPS7A34__AFE_EN

SYS_FAULTNS__AFEAGND

FLOATING RECORDING RAILS

J60006

SYS_VMEAS12B__MON_VREF

SYS_TS1A212__MON_VMID

SYS_SENSE2P4__GND

EXISTING MONITOR REFERENCES

J60005

SYS_FEMA8TL__PACK_BUS

power__VSC_P3

power__VSC_N3

SYS_TLV1762__NPVDD5

SYS_SENSE2P4__GND

CONVERTER TEST POINTS

power__PACK_POS

SYS_FEMA8TL__PACK_BUS

input

File: input.kicad_sch

host3

File: host3.kicad_sch

enable_2

File: enable_2.kicad_sch

boost24

File: boost24.kicad_sch

afe3

File: afe3.kicad_sch

sup3

File: sup3.kicad_sch

host5

File: host5.kicad_sch

enable_3

File: enable_3.kicad_sch

Island

File: Island.kicad_sch

afe4

File: afe4.kicad_sch

sup5

File: sup5.kicad_sch

enable

File: enable.kicad_sch

boost15

File: boost15.kicad_sch

afe5

File: afe5.kicad_sch

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/

File: power.kicad_sch

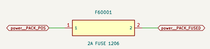
Title: Project SCCI RH S4 / Interfaces and rail handoff

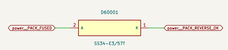
Size: A1 | Date: 2026-10-14 | **Rev: 0.1**

KiCad E.D.A. 10.0.6 | Id: 48/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.











All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/input/
File: input.kicad_sch

Title: Project SCCI RH S4 / Protected pack and input disconnect

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 49/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.

















All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/sup3/

File: sup3.kicad_sch

Title: Project SCCI RH S4 / Always-on supervisor 3.3 V

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 50/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.

















All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/sup5/

File: sup5.kicad_sch

Title: Project SCCI RH S4 / Always-on supervisor 5 V

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 51/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.

















All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/host3/

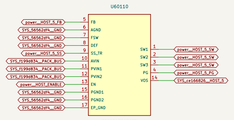
File: host3.kicad_sch

Title: Project SCCI RH S4 / Host logic 3.3 V

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 52/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.





















All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/host5/

File: host5.kicad_sch

Title: Project SCCI RH S4 / Host and module input 5 V

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 53/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.





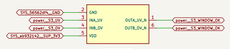














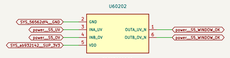






















All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/enable/

File: enable.kicad_sch

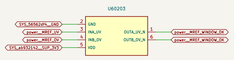
Title: Project SCCI RH S4 / Native battery and startup qualification

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 54/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.









































All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/enable_2/

File: enable_2.kicad_sch

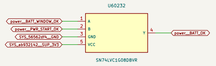
Title: Project SCCI RH S4 / Native battery and startup qualification / 2

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 55/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.



















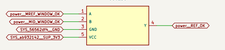


















All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/enable_3/

File: enable_3.kicad_sch

Title: Project SCCI RH S4 / Native battery and startup qualification / 3

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 56/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.























All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/boost15/

File: boost15.kicad_sch

Title: Project SCCI RH S4 / Host 15 V boost

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 57/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.























All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/boost24/

File: boost24.kicad_sch

Title: Project SCCI RH S4 / Stimulation 24 V boost

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 58/80

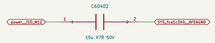
DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.









All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

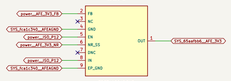
Sheet: /power/island/
File: island.kicad_sch

Title: Project SCCI RH S4 / Floating recording power module

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 59/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.







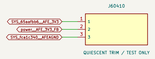












All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/afe3/

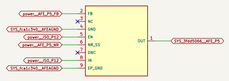
File: afe3.kicad_sch

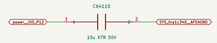
Title: Project SCCI RH S4 / Floating AFE 3.45 V regulator

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 60/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.







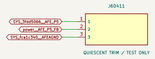












All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/afep/

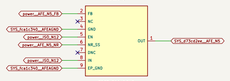
File: afep.kicad_sch

Title: Project SCCI RH S4 / Floating AFE +5.30 V regulator

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 61/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL LOADS / BATTERY AND POWER

25 protected pack, independent supervisor rails, host converters and floating AFE supplies. Digital circuit design, not implant qualification.







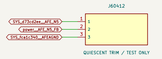












All labels are native electrical connections. PG is diagnostic; full qualification remains the nine independent supervision windows.

Converter shutdown does not discharge boost paths or remove stored energy. Body-facing shutdown remains the separate terminal guards.

Native power: firmware, PCB layout, EMI and physical battery/thermal qualification remain

Project SCCI RH

Sheet: /power/afen/

File: afen.kicad_sch

Title: Project SCCI RH S4 / Floating AFE −5.10 V regulator

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 62/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / MONITORING AND COMPANION

Dedicated raw current/voltage ADC and wired processed-feature companion. Endpoint charge ADCs remain separate.

J70001

HOST RAILS / RAW ADC

J70002

EXISTING ANALOG TAPS

J70003

DEDICATED RAW ADC BUS

monitoring-transport_COMP_5V3

monitoring-transport_COMP_GND

root_2

Files: root_2.kicad_sch

inputs

Files: inputs.kicad_sch

handoff

Files: handoff.kicad_sch

adc

Files: adc.kicad_sch

health

Files: health.kicad_sch

reference

Files: reference.kicad_sch

companion

Files: companion.kicad_sch

Native design: target firmware and PCB verification follow

Project SCCI RH

Sheet: /monitoring-transport/

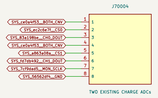
File: monitoring_transport.kicad_sch

Title: Project SCCI RH S4 / Existing package and host endpoints

Size: A1	Date: 2026-10-14
KiCad E.D.A. 10.0.6	**Rev: 0.1**
	Id: 63/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / MONITORING AND COMPANION

Dedicated raw current/voltage ADC and wired processed-feature companion. Endpoint charge ADCs remain separate.







All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native design: target firmware and PCB verification follow

Project SCCI RH

Sheet: /monitoring-transport/root_2/

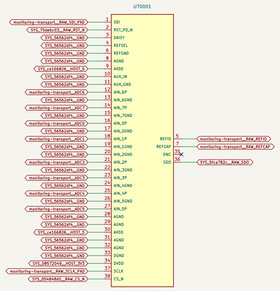
File: root_2.kicad_sch

Title: Project SCCI RH S4 / Existing package and host endpoints / 2

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 64/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / MONITORING AND COMPANION

Dedicated raw current/voltage ADC and wired processed-feature companion. Endpoint charge ADCs remain separate.



All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native design: target firmware and PCB verification follow

Project SCCI RH

Sheet: /monitoring-transport/adc/

File: adc.kicad_sch

Title: Project SCCI RH S4 / Dedicated eight-channel raw conversion

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 65/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / MONITORING AND COMPANION

Dedicated raw current/voltage ADC and wired processed-feature companion. Endpoint charge ADCs remain separate.



















All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native design: target firmware and PCB verification follow

Project SCCI RH

Sheet: /monitoring-transport/reference/

File: reference.kicad_sch

Title: Project SCCI RH S4 / independent ADC reference and bypass

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 66/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / MONITORING AND COMPANION

Dedicated raw current/voltage ADC and wired processed-feature companion. Endpoint charge ADCs remain separate.

































All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native design: target firmware and PCB verification follow
Project SCCI RH
Sheet: /monitoring-transport/inputs/
File: inputs.kicad_sch

Title: Project SCCI RH S4 / Raw current and scaled voltage filtering

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 67/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / MONITORING AND COMPANION

Dedicated raw current/voltage ADC and wired processed-feature companion. Endpoint charge ADCs remain separate.









All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native design: target firmware and PCB verification follow

Project SCCI RH

Sheet: /monitoring-transport/health/

File: health.kicad_sch

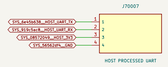
Title: Project SCCI RH S4 / Divided power observations

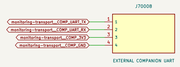
Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 68/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / MONITORING AND COMPANION

Dedicated raw current/voltage ADC and wired processed-feature companion. Endpoint charge ADCs remain separate.















All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native design: target firmware and PCB verification follow

Project SCCI RH

Sheet: /monitoring-transport/companion/

File: companion.kicad_sch

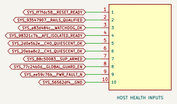
Title: Project SCCI RH S4 / Isolated wired processed-feature companion

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 69/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / MONITORING AND COMPANION

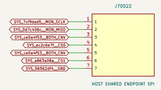
Dedicated raw current/voltage ADC and wired processed-feature companion. Endpoint charge ADCs remain separate.











All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native design: target firmware and PCB verification follow

Project SCCI RH

Sheet: /monitoring-transport/handoff/

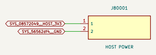
File: handoff.kicad_sch

Title: Project SCCI RH S4 / Charge ADC and health host handoff

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 70/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / nRF5340 CONTROLLER CARRIER

46 actual GPIO, explicit common CNV/rearm and physical 32-bit health/readback chain. Radio remains disabled.





processor

File: processor.kicad_sch

handoff

File: handoff.kicad_sch

defaults

File: defaults.kicad_sch

power

File: power.kicad_sch

handoff_2

File: handoff_2.kicad_sch

defaults_2

File: defaults_2.kicad_sch

sideband

File: sideband.kicad_sch

handoff_3

File: handoff_3.kicad_sch

defaults_3

File: defaults_3.kicad_sch

Native module carrier; physical execution and assembly qualification remain

Project SCCI RH

Sheet: /controller-carrier/

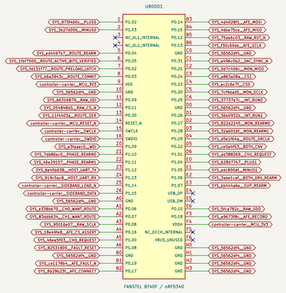
File: controller_carrier.kicad_sch

Title: Project SCCI RH S4 / Controller carrier / interface index

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 71/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / nRF5340 CONTROLLER CARRIER

46 actual GPIO, explicit common CNV/rearm and physical 32-bit health/readback chain. Radio remains disabled.



All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native module carrier; physical execution and assembly qualification remain

Project SCCI RH

Sheet: /controller--carrier/processor/

File: processor.kicad_sch

Title: Project SCCI RH S4 / BT40F / actual nRF5340 physical pads

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 72/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / nRF5340 CONTROLLER CARRIER

46 actual GPIO, explicit common CNV/rearm and physical 32-bit health/readback chain. Radio remains disabled.

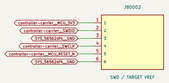














All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native module carrier; physical execution and assembly qualification remain

Project SCCI RH

Sheet: /controller-carrier/power/

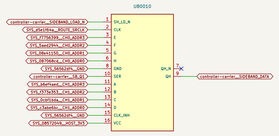
File: power.kicad_sch

Title: Project SCCI RH S4 / Module normal-voltage supply and SWD

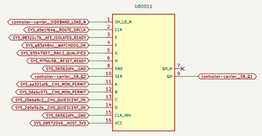
Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 73/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / nRF5340 CONTROLLER CARRIER

46 actual GPIO, explicit common CNV/rearm and physical 32-bit health/readback chain. Radio remains disabled.









All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native module carrier; physical execution and assembly qualification remain

Project SCCI RH

Sheet: /controller-carrier/sideband/

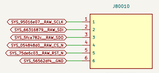
File: sideband.kicad_sch

Title: Project SCCI RH S4 / Four physical 165 devices / parallel observation

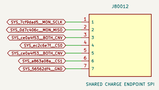
Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 74/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / nRF5340 CONTROLLER CARRIER

46 actual GPIO, explicit common CNV/rearm and physical 32-bit health/readback chain. Radio remains disabled.









All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native module carrier; physical execution and assembly qualification remain

Project SCCI RH

Sheet: /controller-carrier/handoff/

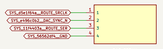
File: handoff.kicad_sch

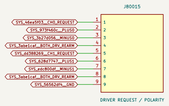
Title: Project SCCI RH S4 / Matched peripheral handoff connectors

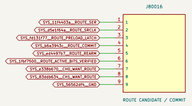
Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 75/80

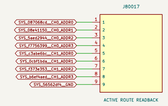
DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / nRF5340 CONTROLLER CARRIER

46 actual GPIO, explicit common CNV/rearm and physical 32-bit health/readback chain. Radio remains disabled.









All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native module carrier; physical execution and assembly qualification remain

Project SCCI RH

Sheets: /controller--carrier/handoff_2/

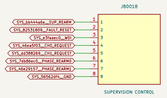
File: handoff_2.kicad_sch

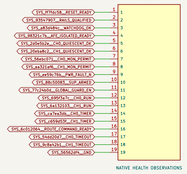
Title: Project SCCI RH S4 / Matched peripheral handoff connectors / 2

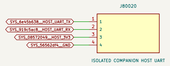
Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 76/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / nRF5340 CONTROLLER CARRIER

46 actual GPIO, explicit common CNV/rearm and physical 32-bit health/readback chain. Radio remains disabled.







All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native module carrier; physical execution and assembly qualification remain

Project SCCI RH

Sheet: /controller-carrier/handoff_3/

File: handoff_3.kicad_sch

Title: Project SCCI RH S4 / Matched peripheral handoff connectors / 3

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 77/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / nRF5340 CONTROLLER CARRIER

46 actual GPIO, explicit common CNV/rearm and physical 32-bit health/readback chain. Radio remains disabled.





























All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native module carrier; physical execution and assembly qualification remain

Project SCCI RH

Sheet: /controller--carrier/defaults/

File: defaults.kicad_sch

Title: Project SCCI RH S4 / Passive reset defaults / explicit recovery

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 78/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / nRF5340 CONTROLLER CARRIER

46 actual GPIO, explicit common CNV/rearm and physical 32-bit health/readback chain. Radio remains disabled.





























All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native module carrier; physical execution and assembly qualification remain

Project SCCI RH

Sheets: /controller-carrier/defaults_2/

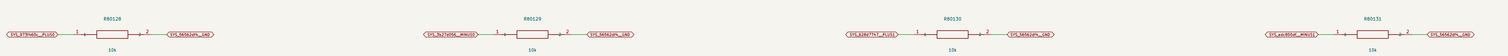
File: defaults_2.kicad_sch

Title: Project SCCI RH S4 / Passive reset defaults / explicit recovery / 2

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 79/80

DIGITAL SCCI ENGINEERING / ARTIFICIAL SIGNALS / nRF5340 CONTROLLER CARRIER

46 actual GPIO, explicit common CNV/rearm and physical 32-bit health/readback chain. Radio remains disabled.



All labels are native electrical connections. Digital artificial-load interface; no clinical, chronic or body-radio qualification.

Hardware permissions and terminal guards remain independent of transport. Loss of data rejects the observation.

Native module carrier; physical execution and assembly qualification remain

Project SCCI RH

Sheet: /controller--carrier/defaults_3/

File: defaults_3.kicad_sch

Title: Project SCCI RH S4 / Passive reset defaults / explicit recovery / 3

Size: A1	Date: 2026-10-14	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 80/80